_____ 8802-3/802.3 REVISION REQUEST +-----+ DATE: 5th March, 2000 NAME: David Drumm COMPANY/AFFILIATION: 3Com ADDRESS: Valley Forge 2435 Blvd. of the Generals, Norristown PA. 19403 PHONE: (610)-635-0100 FAX: E-MAIL: David_Drumm@3com.com REQUESTED REVISION: STANDARD: IEEE Std 802.3ab-1999 CLAUSE NUMBER: 40.3.1.3.3 CLAUSE TITLE: Generation of bits Sc_ n [7:0] PROPOSED REVISION TEXT: It is believed that the text: The four bits Sc_ n [7:4] are defined as Sc _n [7:4] = Sx_ n [3:0] if (tx_enable_ n = 1) [0 0 0 0] else should read: The four bits Sc_ n [7:4] are defined as Sc _n [7:4] = Sx_ n [3:0] if $(tx_enable_{n-2} = 1)$ [0 0 0 0] else RATIONALE FOR REVISION: While at t = n and t = n-1, SSD1 and SSD2 are being sent, respectively, Table 40-1 seems to imply that $Sd_n[6:8]$ should equal [0 0 0]. It is believed that the only way to ensure that $Sd_n[6:8] = [0 \ 0 \ 0]$ is to have $Sc_n[7:4] = [0 \ 0 \ 0 \ 0].$ IMPACT ON EXISTING NETWORKS: None, it is believed that an implementation that meets the text of the standard would not operate correctly. -----+ Please attach supporting material, if any Submit to:- Geoffrey O. Thompson, Chair IEEE 802.3 Nortel Networks, Inc. M/S SC5-02 4401 Great America Parkway P. O. Box 58185 Santa Clara, CA 95052-8185 USA Phone: +1 408 495 1339 FAX: 988 5525 E-Mail: geoff_thompson@baynetworks.com +----- For official 802.3 use -----+ REV REQ NUMBER: 1030 DATE RECEIVED: 5th March, 2000 EDITORIAL/TECHNICAL ACCEPTED/DENIED BALLOT REQ'D YES/NO COMMENTS: Published IEEE Std 802.3-2002 +-----For information about this Revision Request see http://www.ieee802.org/3/maint/requests/revision_history.html#REQ1030

Comment from Sailesh Rao on proposed change:-

Sent by:	"Rac), Sai	llesh"	<saile< th=""><th>esh.rao@ir</th><th>ntel</th><th>.com></th><th></th><th></th><th></th></saile<>	esh.rao@ir	ntel	.com>			
Subject:	RE:	IEEE	Mainte	nance	Revision	to	clause	40	PCS	code

All:

Here is my response to the comment:

The commenter has a valid concern that since $Sc_n[7:4]$ is defined as

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Sc_n[7:4] = Sx_n[3:0] if (tx_enable\{n\} = 1)
[0 0 0 0] else
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in Section 40.3.1.3.3, the bits Sd_n[6:7] need not be [00] during the encoding of SSD1 and SSD2. This renders the definition of SSD1 and SSD2 in Table 40.1 incomplete, since at a minimum, the entries for SSD1 and SSD2 should have been repeated across the 4 columns of this table.

The resolution offered by the commenter is a simpler alternative for clarifying the definition of the SSD1 and SSD2 encoding. I recommend that we accept the resolution.

Since the convolutional encoder states, $cs_n[0:2]$, are defined to be [000] in Section 40.3.1.3.4 during the encoding of SSD1 and SSD2, the trellis code already requires that both SSD1 and SSD2 be encoded from subset D0, regardless of the state of Sd_n[6:7]. Thus, it is very unlikely that the proposed change to Clause 40 has any effect on existing implementations.

Regards, Sailesh.