8802-3/802.3 REVISION REQUEST 1114

DATE: 17th September, 2003
NAME: Peter Bradshaw
COMPANY/AFFILIATION: BitBlitz Communications
E-MAIL: pbradshaw@bitblitz.com

REQUESTED REVISION:
STANDARD: IEEE Std. 802.3ae-2002
CLAUSE NUMBER: 45.2.5.8
CLAUSE TITLE: 10G DTE XGXS lane status register (Register 5.24)

PROPOSED REVISION TEXT:

In 45.2.5.8:

REPLACE: in Table 45-58, replace 5.24.10:4 by 5.24.9:4, and add a new row for 5.24.10 defining it as ignored.

For details see attached draft.

RATIONALE FOR REVISION:

Loopback is optional for a PHY XS device (45.2.4.1.2) (advertised in bit 4.24.10), and mandatory for a DTE XS device (45.2.5.1.2), where the 5.24.10 bit must be 0*. These awkward inconsistencies (a PHY XGXS and a DTE XGXS are otherwise identical, except for Device Address) are enhanced by the addition of the CX4 PMA/PMD, since the functional differences between a CX4 PMA/PMD/PCS device and a DTE XGXS device are mainly some changes to the output and input levels and the SIGNAL_DETECT function, the required register Device Address value changes, and the loopback function and advertising bit scrambling. Thus an implementor must take special steps to return 5.24.10 as a 0, while returning 4.24.10 as a 1. In addition, many LX4 and (future) CX4 devices are likely to use a structure essentially identical to an XGXS device within their signal flow, and may include this kind of loopback.

Allowing the 5.24.10 bit to optionaly be a 1, so that a device that can implement both PHY XGXS and DTE XGXS need not change this status bit when changing device addresses. This makes the design easier and more flexible*.

*Comments on the comment: a small side bet says that any plausible compliant XGXS devices will actually have this loopback capability and bit, and will have had to hide it somewhere in a vendor-specific register or in some other way.

IMPACT ON EXISTING NETWORKS:

Present conforming devices would be allowed to keep this bit a 0, but it would be recommended that it be a 1. Hosts knowing that they have a DTE

XS device are unlikely to even bother to check the bit before turning on loopback, since it is mandatory.

Please attach supporting material, if any	
Submit to:- Bob Grow, Chair IEEE 802.3	
E-Mail: Bob.Grow@intel.com	
+------- For official 802.3 use ----------+	
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For information about this Revision Request see -	
http://www.ieee802.org/3/maint/requests/revision_history.html#REQ1114	

45.2.5.8 10G DTE XGXS lane status register (Register 5.24)

Change the Table 45-59 of subclause 45.2.5.8 as follows:.

Table 45–59—10G DTE XGXS lane status register bit definitions

Bit(s)	Name	Description	R/W[a]
5.24.15:13	Reserved	Ignore when read	RO
5.24.12	DTE XGXS lane alignment status	1 = DTE XGXS receive lanes aligned 0 = DTE XGXS receive lanes not aligned	RO
5.24.11	Pattern testing ability	1 = DTE XGXS is able to generate test patterns 0 = DTE XGXS is not able to generate test patterns	RO
5.24.10	Ignored	Value 0 or 1, writes ignored	RO
5.24.9~~10~~:4	Reserved	Ignore when read	RO
5.24.3	Lane 3 sync	1 = Lane 3 is synchronized 0 = Lane 3 is not synchronized	RO
5.24.2	Lane 2 sync	1 = Lane 2 is synchronized 0 = Lane 2 is not synchronized	RO
5.24.1	Lane 1 sync	1 = Lane 1 is synchronized 0 = Lane 1 is not synchronized	RO
5.24.0	Lane 0 sync	1 = Lane 0 is synchronized 0 = Lane 0 is not synchronized	RO

[a]RO = Read Only