8802-3/802.3 REVISION REQUEST 1164

DATE: 30th March, 2005
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REQUESTED REVISION:
- STANDARD: IEEE Std. 802.3af-2003
- CLAUSE NUMBER: Figure 33C.11
- CLAUSE TITLE: Align informative figure with normative text

PROPOSED REVISION TEXT:

1. Change Figure 33C.11 as follows:
1.1 move the vertical dashed line to cross the horizontal 2.8VDC dashed line at the beginning of the detection signal.
1.2 move the vertical dashed line at the end of the detection period to a location within the higher section of the detection signal curve.
1.3 Move vertical dashed lines of classification voltage to clearly show classification time interval.
1.4 Locate the labels "T0", "S1=Closed" and T1 at the correct locations shown in the attached drawing.
1.5 Y axis label of the drawing should be replaced with "Vport"
1.6 Delete Vport(cc) horizontal dashed line and Vport(cc) label.
1.7 Show in the drawing that the example shown is one of many possibilities by marking the parts that may be different by dashed line.
1.8 Move Iport curve zero point to line up with Zero voltage of Vport at turn on point as shown.
1.9 Add text box "Dashed portion of the wave forms is undefined"
1.10 Change the text in the upper right corner box from:
" Disconnect detection function starts here" To: "Disconnect detection function starts here or in lower current according the MPS method being used."
1.11 Change the following text from: "... After this point, detection results must be reset and new detection cycle must be generated."
To: "... After this point, detection results must be reset and new detection cycle may be generated."

RATIONALE FOR REVISION:

See attached corrected drawing of 33C.11, Changes are marked with red color.

1.1 The current drawing shows that the vertical dashed line that specify the start of the detection time are crossing the detection voltage at zero voltage which is an error according to table 33-2 item 3. It should cross at the 2.8VDC horizontal dashed line.
1.2 The end of the detection voltage can be anywhere as long as Vvalid per table 33 item 3 is kept.
1.3.The vertical lines that shows the classification time duration should be aligned to the min classification voltage.
1.4 The label "T0" and S1=Closed" are located at the same timing point which is an error. T0 is the beginning of the detection time and S1 is the time that S1 in the test setup is closed which happen before T0 in the general case. The label T1 should show the end of the detection timing.
1.5 The label of the Y axis of the drawing "Voltage" should be replaced with Vport which is actually the signals tested at the port.
1.6 The label "Vport (cc)" adds no information to the drawing and should be deleted. "(cc)" is the port nodes according drawing 33C.12 which adds no information.
1.7 Detection and classification signals vs time may be different than the example shown in the drawing and it is convenient to show it by adding the dashed lines to the locations were it is allowed to be different by the spec.
1.8 Iport can't be > 0 while Vport during startup =0. Need to synchronize the voltage and current drawings.
1.9 The drawing meant to illustrate the timing between events that was specified in the standard. Undefined parts were drawn with dashed line.
1.10 Disconnect detection starts when the PSE starts powering the port. The exact point is function of the MPS method being used.
1.11 The use of "must" is incorrect since delay between detections is not specified.

Although figure 33C.11 is in the informative part, it will be helpful for the reader to synchronize the drawing to the spec to avoid confusion which.

IMPACT ON EXISTING NETWORKS:

No impact. It is all editorial and informative at the informative section.

Please attach supporting material, if any		
Submit to:- Bob Grow, Chair IEEE 802.3		
E-Mail: Bob.Grow@intel.com		
+------- For official 802.3 use ----------+		
REV REQ NUMBER: 1164		
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For information about this Revision Request see -		
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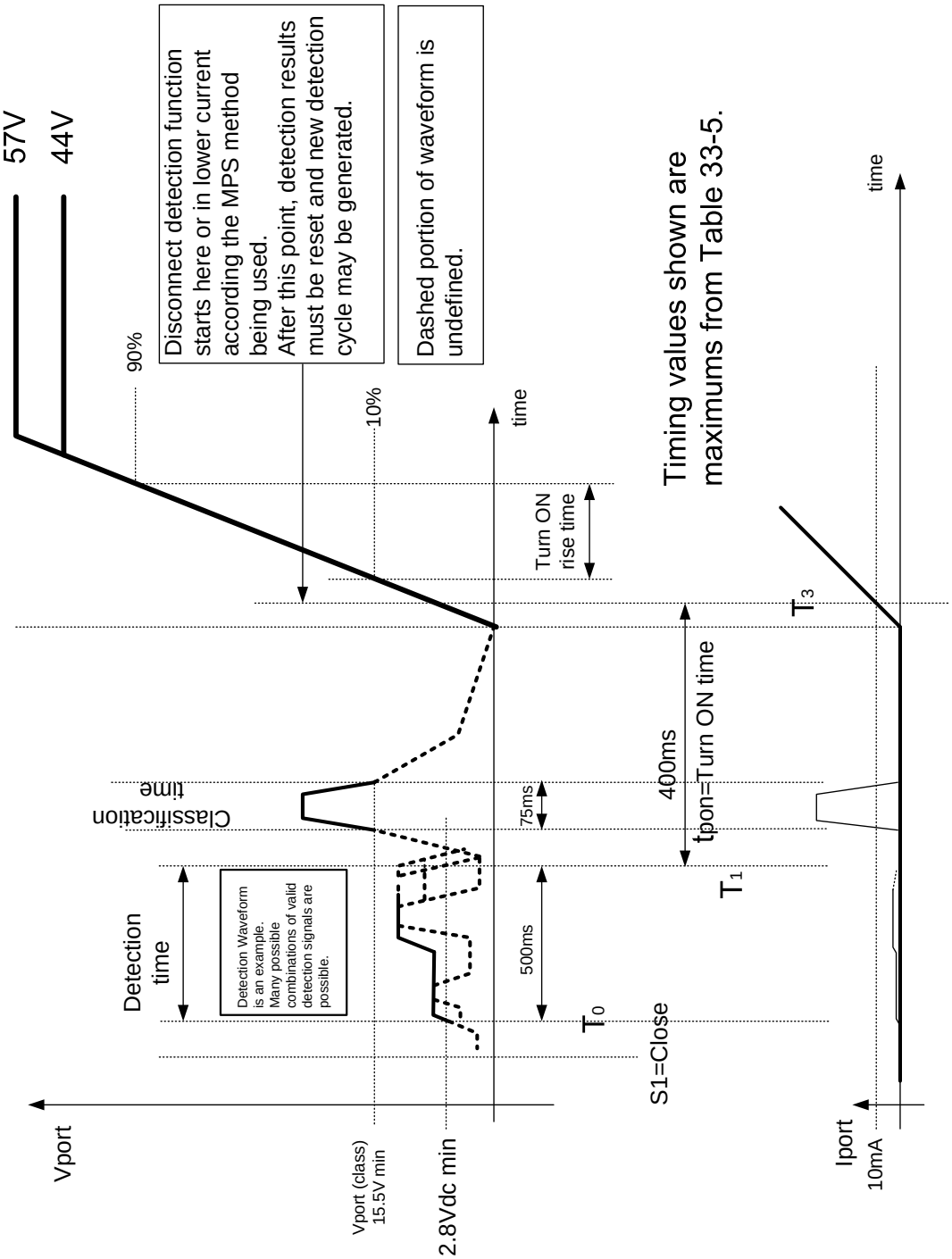
57V
44V
Disconnect detection function starts here or in lower current according the MPS method being used.
After this point, detection results must be reset and new detection cycle may be generated.
Dashed portion of waveform is undefined.
90%
10%
time
Turn ON rise time
Timing values shown are maximums from Table 33-5.
Classification time
Detection time
Detection Waveform is an example. Many possible combinations of valid detection signals are possible.
75ms
500ms
400ms
tpon=Turn ON time
T0
T1
T3
S1=Close
Vport
Vport (class) 15.5V min
2.8Vdc min
Iport
10mA
time