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| 8802-3/802.3 REVISION REQUEST 1170 |  
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DATE: 15th Sept, 2005  
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REQUESTED REVISION:  
STANDARD: IEEE802.3-2005  
CLAUSE NUMBER: 33.2.8.1  
CLAUSE TITLE: Output voltage

PROPOSED REVISION TEXT:

Add the following text to 33.2.8.1 after the end of the 2nd line:

Vport voltage should be within 44V to 57V range under the load conditions as specified in table 33-5 item 8.

Output voltage may be lower than 44V under the load conditions of table 33-5 item 10.

See figure 33C.6.

In startup mode the PSE supplies a limited current as defined by table 33-5 item 5 for a limited time defined by 33.2.8.5 and table 33-5 item 11 that charges the PD input capacitance, causing Vport to ramping up until output voltage reaches its steady state per items 1 and 2 in table 33-5.

RATIONALE FOR REVISION:

The additional text meant to clarify the outcome of table 33-5 items 8 and 10 as described in figure 33C.6.

Table 33-5 item 8: In this condition, Iport may reach to 400mA for a limited time duration and Vport is still keep its operating voltage range in order to allow dynamic load change up to 400mA in the PD per table 33-12 item 4.

Table 33-5 item 10: In this condition Vport may drops to a voltage of  $ILIM \cdot RLOAD$  while RLOAD is the PSE load as defined by the PD specifications. Due to the fact that  $ILIM \gg 350mA$  then Vport during short circuit condition may be lower than 44V.

During startup the PSE is charging the PD DC/DC input cap through a current source or other dissipative element until steady state is reached.

IMPACT ON EXISTING NETWORKS:

None.

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| Please attach supporting material, if any
| Submit to:- Bob Grow, Chair IEEE 802.3
|           E-Mail: Bob.Grow@intel.com
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|           +----- For official 802.3 use -----+
|           | REV REQ NUMBER: 1170
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| For information about this Revision Request see -
| http://www.ieee802.org/3/maint/requests/revision\_history.html#REQ1170
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