DATE: 9/27/2016
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REQUESTED REVISION:
STD: 802.3-2015
CLAUSE NUMBER: 91
CLAUSE TITLE: Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 100GBASE-R PHYs

PROPOSED REVISION TEXT:
Proposal is to modify the FEC synchronization state diagram to add a check for correct AMs after lock is achieved. This protects against the AMs moving (for example in an OTN Network) and this state diagram not noticing and remaining in lock. Similar changes were made to 802.3bs in draft 2.1 due to comment #67 against draft 2.0.

Add the following sentence at the end of the description for the restart_lock variable definition in clause 91: "It is also set to true when 5 Alignment Markers in a row fail to match (5_BAD state) if the optional states are supported in the FEC synchronization process."

Add this new variable in clause 91: "amp_bad_count
Counts the number of consecutive alignment markers that don't match the expected values for a given FEC lane if the optional states are supported in the FEC synchronization process."

See the attached supporting material for the proposed changes to the State diagram.

Add the following PIC:
SD6, FEC synchronization enhancement, 91.5.4.3, Check AMs after synchronization is achieved per Figure 91-8, O, Yes[] No[]

RATIONALE FOR REVISION:
This improves the robustness of the RS-FEC sublayer when used in an application that includes an OTN network (or similar). See http://www.ieee802.org/3/bs/public/16_09/gustlin_3bs_01_0916.pdf for more background.

IMPACT ON EXISTING NETWORKS:
No impact, this is added as an optional part of the standard.
Please attach supporting material, if any

Submit to: David Law, Chair IEEE 802.3
and copy: Adam Healey, Vice-Chair IEEE 802.3

At:
E-Mail: stds-802-3-maint-req@ieee.org

----- For official 802.3 use -----
REV REQ NUMBER: 1299
DATE RECEIVED: 3rd August, 2016
EDITORIAL/TECHNICAL
ACCEPTED/DENIED
BALLOT REQ'D YES/NO
COMMENTS:

For information about this Revision Request see -
http://www.ieee802.org/3/maint/requests/revision_history.html#REQ1299
Figure 91-8—FEC synchronization state diagram

NOTE 1—States inside the dotted box and transition A are optional.