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2  |                8802-3/802.3 REVISION REQUEST                |
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4  DATE: 21 May 2017
5  NAME: Andrew Gardner
6  COMPANY/AFFILIATION: Analog Devices (formerly Linear Technology)
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8
9  REQUESTED REVISION:
10     STANDARD: 802.3bu
11     CLAUSE NUMBER: 104.4.4.1
12     CLAUSE TITLE: Detection probe requirements
13     PROPOSED REVISION TEXT:
14
15     Change the max limit for item 5 in Table 104-3 PSE PI detection state
16     electrical output requirements from 200nF to 2.64uF. 2.2uF+20% =
17     2.64uF.
18
19     RATIONALE FOR REVISION:
20
21     The 200nF maximum limit on a PSE's Cout is limiting. The current maximum
22     limit in some common circuit configurations can cause stability issues.
23     The attached analysis demonstrates that the proposed change does not
24     create the potential for one PSE to detect another PSE as a valid PD.
25     In addition, since no other detection parameters are affected, there is
26     no impact on interoperability of existing PoDL networks.
27
28     IMPACT ON EXISTING NETWORKS:
29
30     No impact is anticipated. Networks that meet the existing spec will also
31     be able to meet the relaxed specification.
32
33  +-----+
34  | Please attach supporting material, if any                      |
35  | Submit to:- David Law, Chair IEEE 802.3                      |
36  | and copy:- Adam Healey, Vice-Chair IEEE 802.3              |
37  |                                                              |
38  | At:- E-Mail: stds-802-3-maint-req@ieee.org                  |
39  |                                                              |
40  |           +----- For official 802.3 use -----+         |
41  |           | REV REQ NUMBER: 1308                          |         |
42  |           | DATE RECEIVED: 21st May 2017                  |         |
43  |           | EDITORIAL/TECHNICAL                          |         |
44  |           | ACCEPTED/DENIED                               |         |
45  |           | BALLOT REQ'D      YES/NO                      |         |
46  |           | COMMENTS:                                       |         |
47  +-----+
48  | For information about this Revision Request see -           |
49  | http://www.ieee802.org/3/maint/requests/revision\_history.html#REQ1308 |
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# 1 Analysis of Proposed Change to $C_{out}$

## 2 Maximum Limit in Table 104-3

### 3 Objective

4 To demonstrate that the output capacitance ( $C_{out}$ ) maximum limit on a PSE in Table 104-3 can be  
 5 increased from 200nF to 2.64 $\mu$ F during detection without creating the potential for a PSE to  
 6 detect another PSE as a valid PD.

### 7 Justification

8 The existing PSE 200nF  $C_{out}$  max limit in Table 104-3 is limiting and can cause stability issues with  
 9 some common PoDL circuit configurations.

### 10 Analysis of a PSE during DETECTION

11 A PSE that implements detection is required to meet the electrical specifications in Table 104-3  
 12 (shown below). In addition, a PSE is required to have an output with attributes that will prevent it  
 13 from being detected as a valid PD by another PSE (see 104.4.6 PSE output requirements).

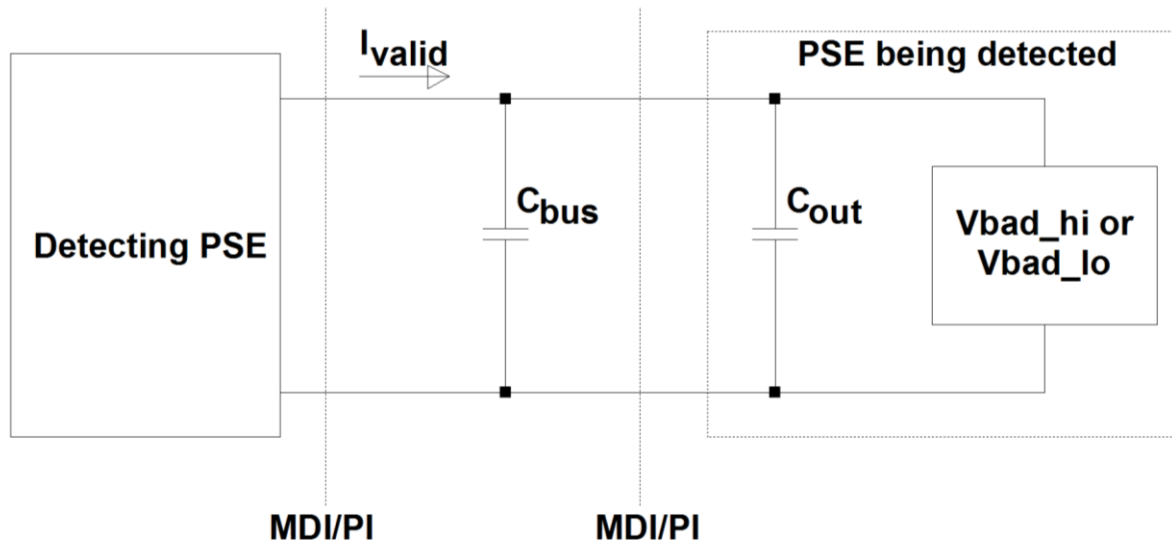
**Table 104–3—PSE PI detection state electrical output requirements**

Item	Parameter	Symbol	Unit	Min	Max	Additional information
1	Open circuit voltage	$V_{OC}$	V	4.75	5.5	
2	Short-circuit current	$I_{SC}$	mA	—	24	
3	Valid test probe current	$I_{valid}$	mA	9	16	
4	Slew rate	$I_{slew}$	A/ms	—	1	
5	Output capacitance during detection	$C_{out}$	nF	—	200	
6	Maximum detection time	$T_{det}$	ms	—	3.11	See 104.4.4
7	Valid PD detection signature range measured at PSE PI	$V_{good\_PSE}$	V	4.05	4.7	See 104.4.4.2
8	Invalid PD detection signature high range measured at PSE PI	$V_{bad\_hi\_PSE}$	V	$V_{oc}-0.05$	—	See 104.4.4.3
9	Invalid PD detection signature low range measured at PSE PI	$V_{bad\_lo\_PSE}$	V	—	3.7	
10	Signature hold timer for validity	$T_{sig\_hold}$	ms	1	—	See 104.4.4.2

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- 1 The  $C_{out}$  maximum limit may be increased from 200nF to 2.64 $\mu$ F without creating the potential for
- 2 one PSE to mis-detect another PSE as a valid PD.



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*Figure 1 – Circuit Model of PSE Detection of another PSE*

5 Figure 1 illustrates a circuit model of a PSE attempting to detect another PSE. Ranges for values of  
6  $I_{valid}$  and  $C_{out}$  are given in Table 104-3.  $C_{bus}$  is constrained to be less than 6nF by Item 19 in Table  
7 104-8 (SCCP electrical requirements).

8 In order to guarantee that a PSE cannot detect another PSE as a valid PD, the total amount of  
9 capacitance seen by the detecting PSE ( $C_{bus}+C_{out}$ ) must be low enough so as to ensure that the  
10 voltage at the MDI/PI of the detecting PSE does not remain in the window  $V_{bad\_lo\_PSE}$  max to  
11  $V_{bad\_hi\_PSE}$  min for more than  $T_{sig\_hold}$  min. The expression for the amount of time spent in the  
12 window,  $t_{bad\_lo\_hi}$ , is given by Equation 1.

13 
$$t_{bad\_lo\_hi} = (V_{bad\_hi\_PSE} - V_{bad\_lo\_PSE}) \times (C_{bus} + C_{out}) / I_{valid} \text{ (Equation 1)}$$

14 The maximum value of  $t_{bad\_lo\_hi}$  occurs when  $V_{bad\_hi\_PSE} = 5.45V$ ,  $V_{bad\_lo\_PSE} = 3.7V$ ,  $I_{valid} = 9mA$ ,  $C_{bus} = 6nF$ ,  
15 and  $C_{out}$  is at the maximum allowed value. Substituting 2.64 $\mu$ F for  $C_{out}$  yields  $t_{bad\_lo\_hi} = 515\mu s$  which  
16 is substantially less than the  $T_{sig\_hold}$  min value of 1ms.

## 17 Conclusion

18 Increasing the maximum limit for  $C_{out}$  from 200nF to 2.64 $\mu$ F in Table 104-3 allows PSEs to be  
19 implemented at lower cost and complexity without creating the potential for one PSE to detect  
20 another PSE as a valid PD.