OIF Liaison to IEEE 802.3 on CEI-112G Project Scopes & Objectives

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Abstract: This presentation provides liaison report on project scope and objectives of CEI-112G-MCM, CEI-112G-VSR, CEI-112G-MR, CEI-112G-LR, to the IEEE 802.3.

CEI-112G MCM Project Scope

- The IA shall define an interface of 1 to N lanes consisting of W wires per lane running at a normalized throughput of up to 58 Gb/s per wire.
  - Total throughput of a lane is W x 58 Gb/s. This is the equivalent throughput density of a differential pair running at 116 Gb/s.
- The IA shall define electrical characteristics and electrical signaling of the lane.
- The IA shall define the applicable data characteristics.
  - Some applications may not have a minimum transition density
  - Some applications may require balanced data
- The IA shall define the compliance channel models that support an organic substrate MCM and other channels with similar characteristics, e.g. up to 1 cm die bump-to-bump with no connectors.
- The IA shall define the interoperability methodologies applicable for the defined signaling method.
- The IA shall not:
  - Define the management interface
  - Define pin assignments
  - Define link negotiation or training protocols

From P6, OIF2017.038.03

CEI-112G MCM Expected Output

- **Project Output:**
  - One or more new clauses for the CEI IA specifying die-to-die interface of 1 to N lanes, each lane consisting of W wires.
  - One or more electrical specifications for lane operation with a normalized throughput density of 58 Gb/s per wire.
  - Reach range: 0 to 1 cm, bump-to-bump

- **Project Requirements:**
  - Support DC coupled path, on-die AC coupling optional
  - Support CMOS-CMOS applications
  - Support CMOS to analog applications
  - This could require separate clauses
  - Bit Error Ratio of 1E-15 or better (high-latency FEC may *not* be used to achieve this)
  - Document constraints of the applications used to derive the channel model specifications.
  - Minimize power (pJ/bit) requirements.

From P7, OIF2017.038.03

CEI-112G-VSR: Project Statement

- **A narrow chip-to-module interface is needed to enable smaller and lower normalized power 112G/lane optical modules.**
- **This project will facilitate an increase in faceplate port density in carrier equipment by a minimum factor of 2, and a decrease in normalized power consumption.**

From P2, OIF2016.315.03

CEI-112G-VSR: Scope

From P3, OIF2016.315.03

- This project will be built on the relevant and appropriate previous 56G CEI projects.
- The Implementation Agreements (IAs) shall define data lane(s) that support bit rates up to 112 Gbps over materials such as Printed Circuit Boards (PCB) or other advanced channel medium for chip-to-module (c2m) interfaces. This implementation agreement is needed to increase the faceplate density over existing modules by at least a factor of 2.
- The IAs shall define the applicable data characteristics (e.g., Modulation, equalization, eye opening).
- The IAs shall define a compliance channel model for a c2m interface including a single connector that will support up to a minimum of 100mm on a host channel, a minimum of 20 mm on a module channel, and up to 1 connector
- The IAs shall not:
  - Define the management interface
  - Define the pin assignments or select a specific connector

CEI-112G-VSR:Project Start Justification 1

- **Project name**
  - CEI-112G-VSR
- **Problem statement**
  - A narrow chip-to-module interface is needed to enable smaller and lower normalized power 112G optical modules.
- **Scope**
  - The project will reuse CEI-56G-VSR materials or other advanced materials when appropriate
  - The IA(s) will define electrical I/O lane(s) that support data rate of 112 Gbps (i.e., 2X of CEI-56G-VSR)
  - The IA(s) will define the output and input compliances based on c2m applications and topologies
  - The IA(s) will support AC coupling
  - The IA(s) will support hot plug
  - The IA(s) will define a test methodology
  - The IA(s) will not define pin assignments nor Management Interface

From P4, OIF2016.315.03

CEI-112G-VSR:Project Start Justification 2

- **Output**
  - One or more clauses added to CEI IA
- **Requirements**
  - IA(s) specifying c2m interfaces of 1 to N lanes, with per lane speed to 112 Gbps
  - Support AC coupling
  - BER of 1e-15 or lower (FEC is allowed to achieve the BER objective)
  - Reach range: up to at least 100 mm host channel, up to at least 20 mm module channel , and up to 1 connector.
  - Definition of compliance test methodology for output and input
  - Document constraints of the c2m applications used to derive the compliance specifications

From P5, OIF2016.315.03

CEI-112G-MR: Scope

- This project will be built on the relevant and appropriate previous 56G CEI and current 112G CEI projects.
- The Implementation Agreements (IAs) shall define data lane(s) that support bit rates up to 112 Gbps over materials such as advanced Printed Circuit Boards (PCB) or other advanced channel medium for chip-to-chip (c2c) interfaces. This implementation agreement is needed to increase the density over existing c2c I/O link by at least a factor of 2.
- The IAs shall define the applicable data characteristics (e.g., modulation, equalization, SNDR, jitter, COM).
- The IAs shall define a compliance channel model for a c2c interface including one connector
- The IAs shall not:
  - Define the management interface
  - Define the pin assignments or select a specific connector

From P4, OIF2017.534.01

CEI-112G-MR: Project Start Justification 1

- Project name
  - CEI-112G-MR
- Problem statement
  - A narrow chip-to-chip interface is needed to enable high density and lower normalized power 112G chip-to-chip applications that matches 112G chip-to-module applications.
- Scope
  - The project will reuse CEI-56G-MR, and CEI-112G-VSR, or other advanced materials when appropriate.
  - The IA(s) will define electrical I/O lane(s) that support data rate from 72 to 116 Gbps (i.e., 2X of CEI-56G-MR).
  - The IA(s) will define the compliance channels with reach up to 500 mm and up to one connector using materials such as advanced Printed Circuit Boards (PCB) or other advanced channel medium, e.g., cables.
  - The IA(s) will support AC coupling.
  - The IA(s) will support hot plug.
  - The IA(s) will define a test methodology.
  - The IA(s) will not define pin assignments nor Management Interface.

From P5, OIF2017.534.01

CEI-112G-MR: Project Start Justification 2

- Output
  - A 112G-MR clause be added to CEI IA
- Requirements
  - IA(s) specifying c2c interfaces of 1 to N lanes, with per lane speed from 72 to 116 Gbps.
  - Reach range: up to at least 500 mm channel length, and up to 1 connector.
  - BER of 1e-15 or lower (FEC is allowed to achieve the BER objective).
  - Support AC coupling.
  - Definition of compliance test methodology for output and input.
  - Definition of compliance methodology for channel.
  - Document constraints of the c2c applications used to derive the compliance specifications

From P6, OIF2017.534.01

CEI-112G-LR: Scope

- This project will be built on the relevant and appropriate previous 56G and 112G CEI projects.
- The resultant Implementation Agreement (IA) shall define data lane(s) that support bit rates up to 112 Gbps over advanced material Printed Circuit Boards (PCB) and twinax cable structures for backplane interfaces. This implementation agreement is needed to increase the backplane bandwidth density over existing backplanes by at least a factor of 2.
- The IA shall define the applicable data characteristics (e.g., modulation, equalization, SNDR, jitter, COM).
- The IA shall not:
  - Define the management interface
  - Define the pin assignments or select a specific connector

From P4, OIF2017.348.01

CEI-112G-LR: Project Start Justification 1

- Project name
  - CEI-112G-LR
- Problem statement
  - A narrow backplane interface is needed to enable high density 112G line cards and equipment chassis. The same channel definition can be applicable to direct attach copper cables.
- Scope
  - The project will reuse CEI-56G-LR and CEI-112G-VSR materials when appropriate
  - The IA will define electrical lane(s) that support data rates from 72 to 116 Gb/s (2X of CEI-56G-LR)
  - The IA shall define the compliance channel models that support a full-sized backplane, e.g. up to 1000 mm with 2 connectors over twinax cable and shorter using advanced material Printed Circuit Boards.
  - The IA will support AC coupling
  - The IA will not define pin assignments nor Management Interface

From P5, OIF2017.348.01

CEI-112G-LR: Project Start Justification 2

- Output
  - IA specifying backplane interfaces of 1 to N lanes, with per lane speed from 72 to 116 Gbps.
  - Reach range: up to at least 1000 mm reach (consisting of media such as twinax cable and/or advanced material printed circuit boards) including line cards, backplane and 2 connectors.
  - Definition of compliance test methodology for output and input
- Requirements
  - Support AC coupling
  - BER of 1e-15 or lower (FEC is allowed to achieve the BER objective).
  - Document constraints of the backplane applications used to derive the compliance specifications

From P6, OIF2017.348.01

Thank You !