P802.3ae TF Logic Track Summary

Ben Brown P802.3ae TF Logic Track Chair 13-July-2000

Blue Book Distribution

- Bob Grow, Intel: "History of the Blue Book"
 - Showed the original 1980 Ethernet Blue Book as generated by Digital, Intel & Xerox
 - Blue Books existed for 100 Mbps and 1000 Mbps Ethernet
- Brad Booth, Intel: "Blue Book Structure"
 - Layers for LAN & WAN, WWDM & Serial
 - Interfaces to be specified (XGMII, XAUI & XBI)
 - Adjacent blocks without specific interfaces (PCS/WIS, PMA/PMD)
 - Describes existing and new clauses
 - Reviewed latest nomenclature for PHY Types
 - Backup slides with possible implementations using standardized functions and interfaces

Presentations

- Shimon Muller, Sun: "Open Loop PHY Rate Control"
 - Entire scheme is more precise in response to Steve Haddock's "IPG & Frame Alignment" proposal
- Shimon Muller, Sun: "Changes to Existing Clauses"
 - Describes changes necessary for the "must haves"
 - Open Loop Rate Control
 - New References, Definitions, Abbreviations and Interfaces
 - Half/ Full Duplex Operation
 - Layer Diagram(s)
 - And the "services to humanity"
 - Speed Independence
 - CRC Passing
 - Document Structure
 - MAN/ WAN "friendliness"
 - Editorial Stuff

- Ed Turner, 3Com: "MDC/MDIO Baseline Proposal"
 - 24 PHYs were tested at UNH IOL for their response to ST=00
 - All 24 ignored them!
- David Law, 3Com: "Management MIB Baseline Proposal"
 - No changes
- Howard Frazier, Cisco: "XGMII Update"
 - Added code point values for I, S, T & E
 - Added some proposed setup & hold numbers
- Steve Haddock, Extreme: "IPG & Frame Alignment"
 - Keep MAC's minimum IPG at 12 bytes (96 bits)
 - Allow RS to "slide" packet to align S with lane 0
 - Results in minimum observed IPG of 9 bytes
 - Maintains minimum average IPG of 12 bytes

- Rich Taborek, nSerial: "XAUI/XGXS"
 - No changes
- Rich Taborek, nSerial: "/Random[A,K]/R/"
 - In support of 12-byte/3 column IPGs
 - Guarantees an /R/ column even in the shortest IPG
 - Statistically guarantees an /A/ and /K/ in 50% of shortest IPGs
- Rick Walker, Agilent: "64b/66b PCS"
 - Clarified bit ordering from 36-bit RS words to 66-bit frames
 - Added preamble to sample test vector
 - Clean up of state machines

- Norival Figueira, Nortel: "WIS Update"
 - Suggestions on how to write the standard by cross-reference to ANSI standards (T1.416-1999)
- Osamu Ishida, NTT: "LSS Proposal"
 - No technical changes
- Stuart Robinson, PMC-Sierra: "XBI Optional Serial PMA Service Interface"
 - Includes some options for REFCLK specs
 - Add waveforms and proposed timing numbers
- Paul Bottorff, Nortel: "SUPI Update"
 - Added detail for lane synchronization and lane deskew
 - Proposed as a PMD Service Interface not a physical instantiation

- Tom Palkert, AMCC: "SUPI"
 - Suggest change to striping from 16 bits to 16 bytes
 - Compatible with proposed OIF VSR protocol

Motions

- Motion #1 included all non-PMD proposals in the Blue Book
 - Through a procedural maneuver, the motion was divided
- Motion #2: "Open Loop PHY Rate Control"
 - 802.3 Voters Y: 113 N: 0 A: 7 **Pass** 100%
- Motion #3: "MDC/MDIO Baseline Proposal"
 - 802.3 Voters Y: 106 N: 0 A: 10 **Pass** 100%
- Motion #4: "Management MIB Baseline Proposal"
 - 802.3 Voters Y: 105 N: 0 A: 9 **Pass** 100%
- Motion #5: "XGMII Update"
 - 802.3 Voters Y: 110 N: 0 A: 4 **Pass** 100%
- Motion #6: "XAUI/XGXS" as modified with /Random[A,K]/R/ proposal (taborek_1_0700)
 - 802.3 Voters Y: 113 N: 0 A: 7 **Pass** 100%
- Motion #7: "64b/66b PCS"
 - 802.3 Voters Y: 104 N: 4 A: 9 **Pass** 96.3%

Motions

- Motion #8: "WIS Update"
 - 802.3 Voters Y: 104 N: 4 A: 9 **Pass** 96.3%
- Motion #9: "LSS Proposal"
 - 802.3 Voters
 Attendees
 Y: 76
 N: 49
 A: 83
 K: 43
 Fail
 63.2%
 60.8%
 - Mation #10: "VPL Optional Sarial DMA Sarvia Interface"
- Motion #10: "XBI Optional Serial PMA Service Interface"
 - 802.3 Voters Y: 85 N: 11 A: 22 **Pass** 88.5%
- Motion #11: "SUPI Update"
 - 802.3 Voters Y: 83 N: 9 A: 25 **Pass** 90.2%
- Motion #12: "IPG & Frame Alignment"
 - 802.3 Voters Y: 92 N: 1 A: 6 **Pass** 98.9%

Thanks!