May 4, 2012

To: David Law and members of IEEE 802.3

Subject: CEI-56G-VSR Project

From: Jonathan Sadler, OIF Technical Committee Chair (jonathan.sadler@tellabs.com)

Dear Mr. Law,
The OIF would like to inform you that we OIF has started a new project to specify a chip-to-module electrical interface with per-lane signaling rates from 39 Gb/s to 56 Gb/s. This is intended to address the fact that by 2014, 28 Gb/s per lane I/O is expected to be a limitation for switch ASIC bandwidth and front-panel port density for some applications.

The project start proposal for the CEI-56G-VSR project is found in document oif2012.088.03 (attached).

Sincerely,

Jonathan Sadler,
OIF Technical Committee Chair (jonathan.sadler@tellabs.com)

Attachment: oif2012.088.03.pdf