Accommodating FEC overhead:
MAC sub-rating vs.
PHY super-rating

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Introduction

- All FEC algorithms have a code rate that is less than unity; that is, they use up bits

- There are two methods to accommodate the added FEC overhead

  - **PHY super-rating:** Increase the PMD line rate

  - **MAC sub-rating:** Reduce the MAC effective data rate

- This presentation lays out the various arguments for and against each alternative

FEC Overhead Allocation

- XGMII rate is fixed at 156.25 MHz

- PHY super-rating means that FEC overhead is allocated below XGMII (i.e., overhead is added to data)

- MAC sub-rating means that FEC overhead is allocated above XGMII (i.e., overhead displaces data)
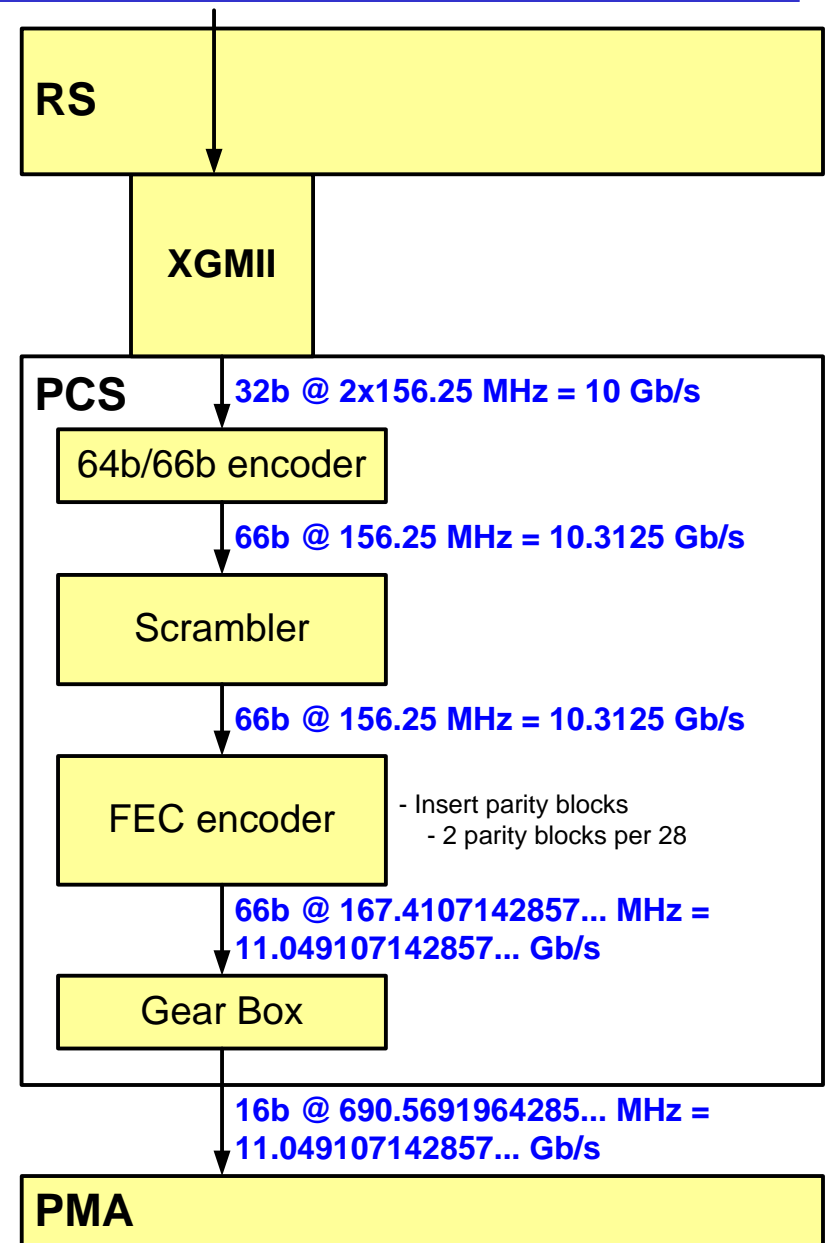
The scale of the issue

- The FEC algorithm has not been selected

- Most proposals have mentioned RS(255,239) as a straw-man choice

  - Super-rated speed would be $1.067\times$nominal

  - Sub-rated speed would be $0.937\times$nominal

- FEC algorithms might go to, say, RS(255, 231)

  - Super-rated speed would be $1.104\times$nominal

  - Sub-rated speed would be $0.906\times$nominal

- So, we're talking about a 7~10% factor

  - Not enough to break a technology

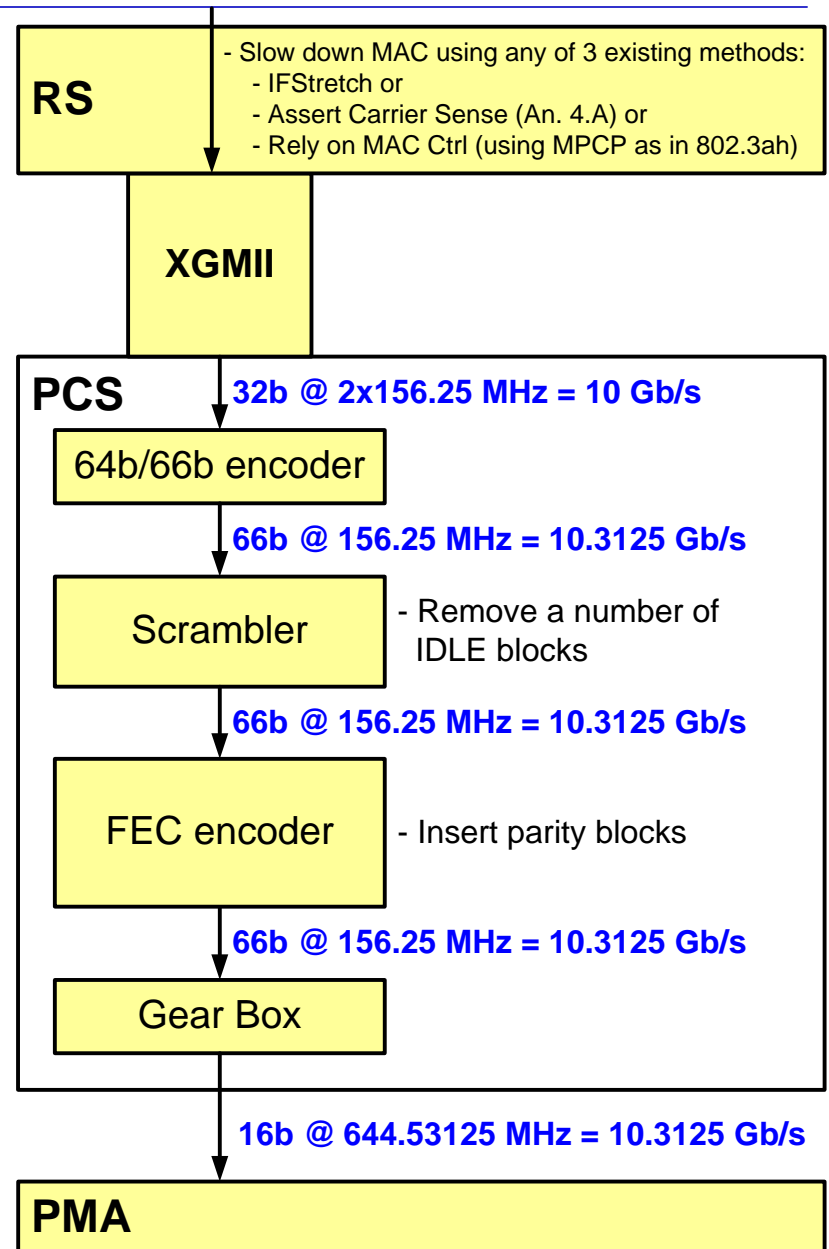 - A 'small signal' analysis should be valid

PHY Super-Rating

- Don't slow down the MAC

- XGMII runs at 156.25 MHz

- FEC inserts extra parity blocks

- In RS(255,239) FEC inserts 2 parity blocks per 28 payload blocks

  - GearBox input clock = 156.25 MHz $\times$ 30/28 = 167.4107142857... MHz

  - PMA clock = 167.4107142857... MHz $\times$ 66/16 = 690.569196428571... MHz

  - PMD rate = 690.569196428571... MHz $\times$ 16 = 11.0491071428571... Gb/s

RS

XGMII

PCS

32b @ 2x156.25 MHz = 10 Gb/s

64b/66b encoder

66b @ 156.25 MHz = 10.3125 Gb/s

Scrambler

66b @ 156.25 MHz = 10.3125 Gb/s

FEC encoder

- Insert parity blocks
  - 2 parity blocks per 28

66b @ 167.4107142857... MHz = 11.049107142857... Gb/s

Gear Box

16b @ 690.5691964285... MHz = 11.049107142857... Gb/s

PMA

MAC Sub-Rating

- Slowing down MAC means inserting more IDLEs between frames (actual MAC and XGMII rates remain the same)

- There exist 3 methods to slow down the MAC:

  1. Inter-frame Stretch (Clause 4)

  2. Carrier Sense (Annex 4A enables using carrierSense to extend deference due to congestion in the PHY)

  3. MPCP frame delay (802.3ah)

- Extra IDLE blocks are removed (marked) before the scrambler.

- FEC encoder inserts matching number of parity blocks

RS

- Slow down MAC using any of 3 existing methods:
  - IFStretch or
  - Assert Carrier Sense (An. 4.A) or
  - Rely on MAC Ctrl (using MPCP as in 802.3ah)

XGMII

PCS

32b @ 2x156.25 MHz = 10 Gb/s

64b/66b encoder

66b @ 156.25 MHz = 10.3125 Gb/s

Scrambler — - Remove a number of IDLE blocks

66b @ 156.25 MHz = 10.3125 Gb/s

FEC encoder — - Insert parity blocks

66b @ 156.25 MHz = 10.3125 Gb/s

Gear Box

16b @ 644.53125 MHz = 10.3125 Gb/s

PMA

PHY Super-Rating

Pros

- The MAC rate is untouched

  – Everything upstream of the PON need not care that there is FEC going on

- Super-rated optics already exist

  – 11.049 Gb/s optics are sold currently

  – Same parts support both rates

- Super-rating is the standard approach in Ethernet for line coding – why not use the same method for FEC?

  – 1.25 Gb/s is the 8b10b code super-rate for 1G

  – 10.3125 Gb/s is the 64b66b code super-rate for 10G

Cons

- Receiver sensitivity is reduced

  – 6.6% over-rate equals 0.3 dB penalty

  – 10.4% over-rate equals 0.4 dB penalty

- Existing 10.3125 Gb/s devices or equipment can't interface to new line rate

- Who needs a full 10G, anyway?

One or two respondents mentioned that the sensitivity impact of super-rating is larger than theory, and is ~1 dB. This can be understood if optics are not optimized, and therefore have insufficient bandwidth for the super-rate. The increased penalty arises from ISI.

MAC Sub-Rating

Pros

- Line Rate remains same as 10GbE

  – Reuse of PMA and PMD components

- Support of FEC optionallity

  – May be not important for 10G PON

- MAC sub-rating was the approach for 1G EPON FEC – why change now?

- Could result in simpler 62.5 MHz clock generation (for asymmetric 10G/1G system)

Cons

- MAC data rate is decreased from standard 10GbE

  – May not be important, as effective user rate has to be reduced anyway due to various other PON overheads

- IPG stretching mechanism must be used

  – Minor complexity issue

  – There are several existing options for this

- PMD reuse is doubtful, since PON loss budget is so different from P2P 10GbE budgets

Additional Thoughts

- A <u>hybrid solution</u> could be considered

    - Super-rating in the downstream, where link budget is more forgiving (perhaps)

    - Sub-rating in the upstream, where the link budget is more stringent

Reaching a Decision

- There are several ways to decide
- On the basis of cost:
  - Which is worse? The Cost premium of super-rated optics, or the Lost revenue due to MAC sub-rating?
- On the basis of 'Style'
  - Architecturally clean, with added cost
  - Pragmatically economic, with complications

Straw Poll

- A preferred method for accommodating FEC overhead is

	All	802.3
• PHY super-rating:	_7__	__7_
• MAC sub-rating:	_40_	_23_
• No opinion/Don't care:	_32_	_23_