INTERNATIONAL TELECOMMUNICATION UNION

TELECOMMUNICATION STANDARDIZATION SECTOR

STUDY PERIOD 2009-2012

COM 15 – LS 292 – E

English only

Original: English

Question(s): 13/15 Geneva, 14-25 February 2011

LIAISON STATEMENT

Source: ITU-T Study Group 15

Title: Copper 10 Gbit/s PHY asymmetry

LIAISON STATEMENT

For action to: IEEE 802.3

For comment to: -

For information to: -

Approval: Agreed to at Study Group 15 meeting (Geneva, 14-25 February 2011)

Deadline: 1 May 2011

Contact: Jean-Loup Ferrant Email: jean-loup.ferrant@calnexsol.com

Contact: Stefano Ruffini Email: stefano.ruffini@ericsson.com

Timing aspects of packet networks is the principal area of focus for ITU-T Q13/15. From Q13/15 perspective the timing includes frequency and time of day(ToD)/phase. A current Q13/15 target for time accuracy after transport over a network is +/-1µs. This error consists of all possible impairments in the network during normal operation. Minimizing asymmetry in the packet propagation delay is a very important item for a proper ToD/phase distribution.

An issue of possible asymmetry between the transmit side and the receive side of a copper 10 GE PHY came recently into the attention of the group.

Special techniques are implemented in the 10 GE PHYs to compensate for radio frequency interference (RFI) coming from copper cable. It appeared that in order to compensate for these impairments, some of 10 GE PHYs incorporate, on Digital Signal Processors, complex signal processing located between analog and digital portion of the receive side. When the link is established, the Rx delay is stable unless the cable length changes.

This digital processing creates asymmetry.

IEEE P802.3bf defines PHY registers containing minimum and maximum path delays for each direction in the PHY.

Q13/15 would greatly appreciate IEEE 802.3 to kindly provide feedback on any of the following:

1. Will the minimum and maximum path delay values in the PHY registers provide accurate information about the delays in each direction, taking the actual active operating mode of the signal processing into consideration or will the values be the absolute minimum and maximum path delays for the PHY, independent of the actual operation mode of the signal processing?
2. Any recommendation on the best way to compensate for the asymmetry.

Q13/15 next meeting where the time and phase synchronization will be discussed is May 2-6, 2011 in Indianapolis, IN, USA.