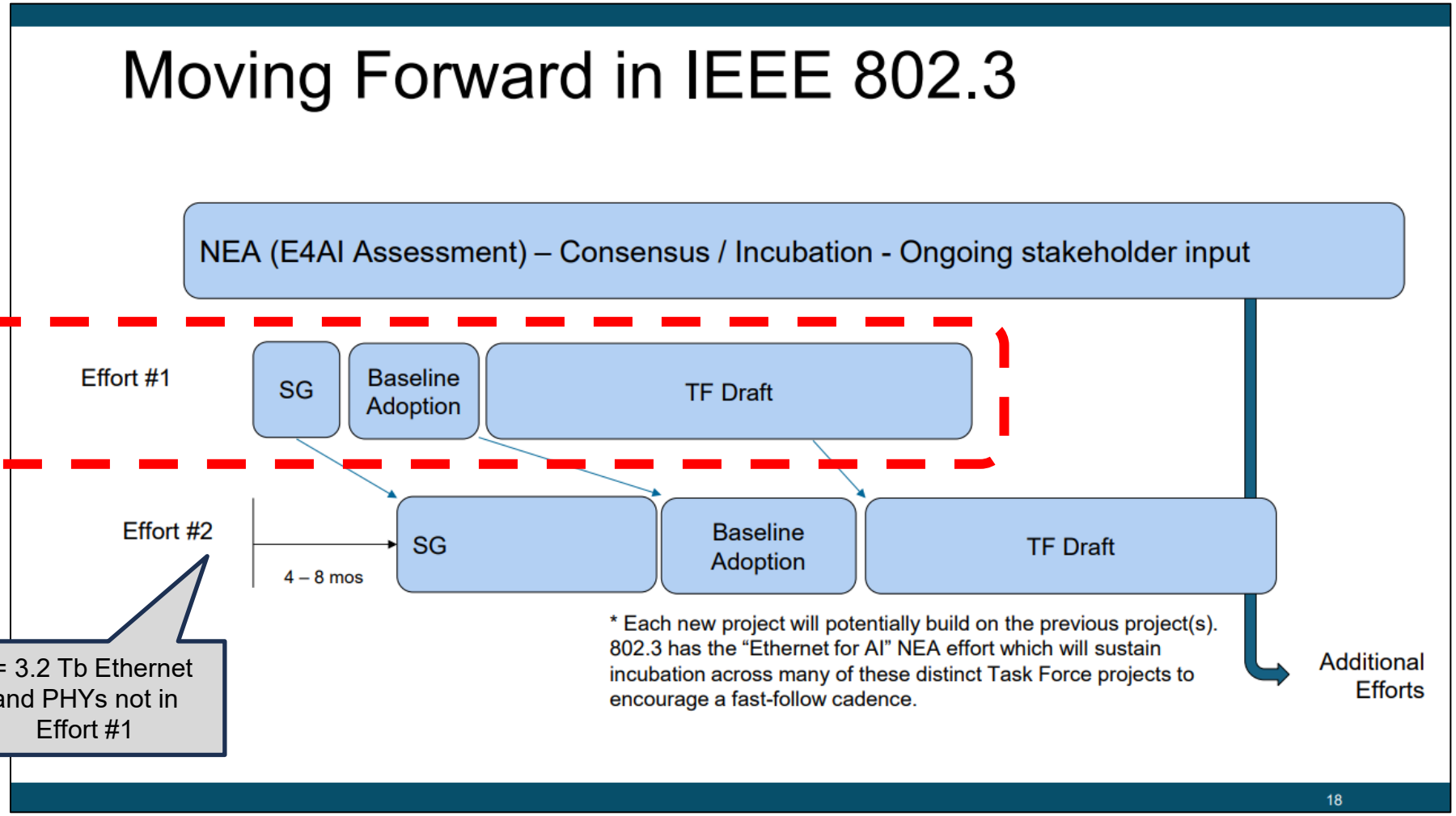
400 Gbps per lane PHYs and Interfaces

Call for Interest (CFI) Opening Report

Kent Lusted, Synopsys

March 2026 Plenary Meeting, Vancouver, BC, Canada

Two Efforts Forming In the Pipeline



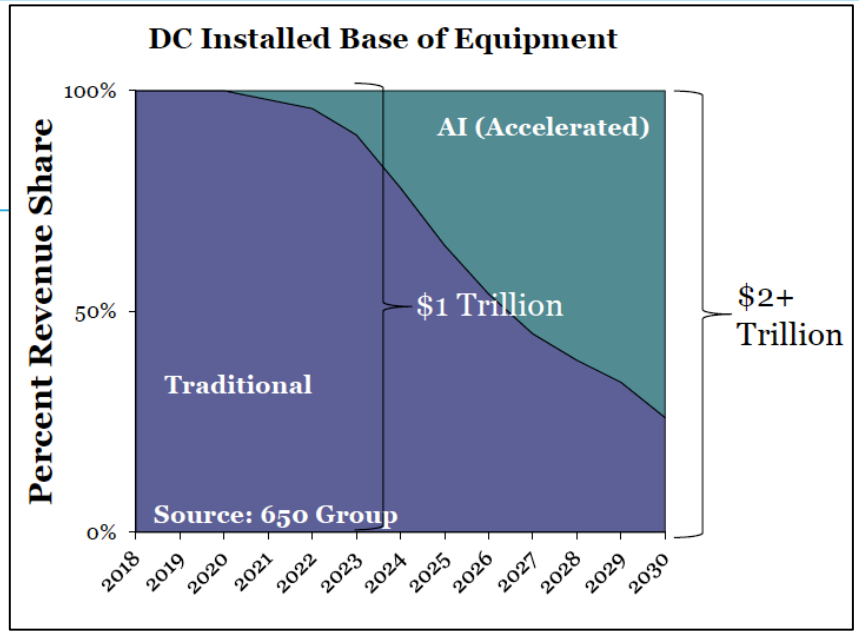
https://www.ieee802.org/3/ad_hoc/E4AI/public/25_0819/dambrosia_e4ai_01_250819.pdf

Overview

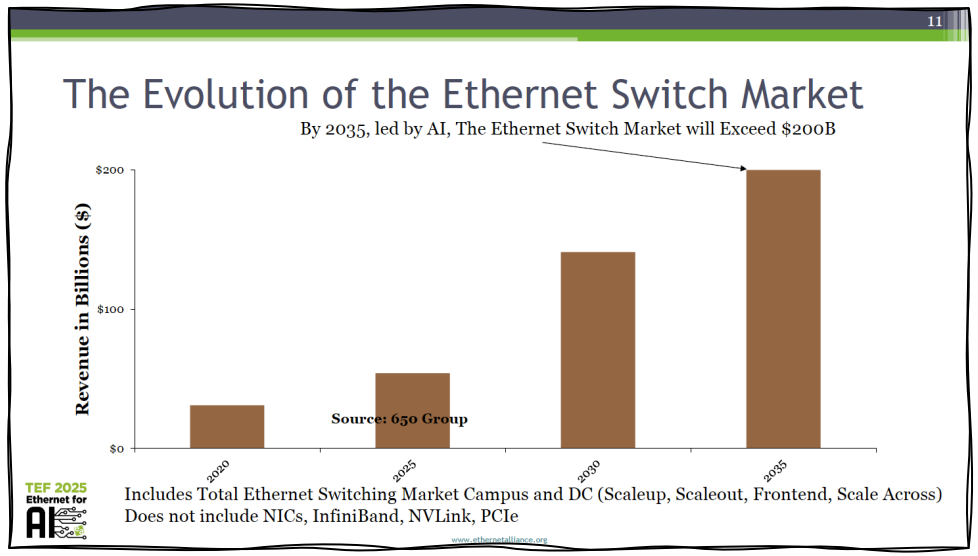
To keep pace with the technology demands necessary to support the projected growth in AI Infrastructure, 400 Gbps/lane data rate PHYs need to be defined in IEEE 802.3

Motivation

- The enormous growth of AI/ML is placing unprecedented **demand on system interconnects and on scaling the bandwidth**, specifically xPU-to-xPU (via switches)
- Ethernet is uniquely positioned to be the building block of choice for AI/ML system interconnects
- The scale of the deployments requires a robust ecosystem to support the volumes.
- In networking, Ethernet wins due to its robust ecosystem and supply chain



Source: Alan Weckel, EA's TEF 2025, "Setting the stage for networking in an AI world"



Source: Alan Weckel, EA's TEF 2025, "Setting the stage for networking in an AI world"

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Many Consortia are Relying on Ethernet

To support the breadth of AI applications, multiple organizations exist:

Ultra Ethernet Consortium

Deliver an Ethernet based open, interoperable, high performance, full-communications stack architecture

ULTRA ACCELERATOR LINK™

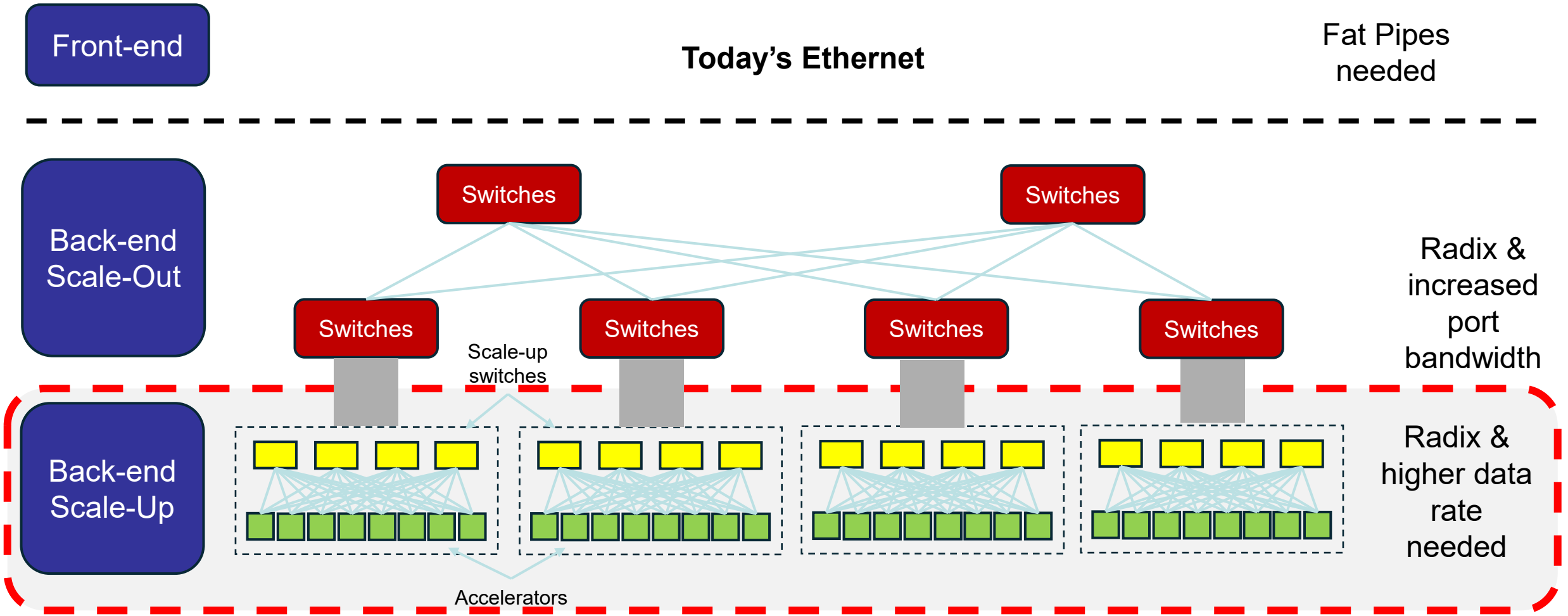
An open, high-bandwidth and low latency interconnect for connecting AI accelerators (such as GPUs) and switches

OPEN Compute Project®

SUE and ESUN build on Ethernet by introducing evolutionary enhancements that improve throughput, latency, and reliability to meet the demands of Scale-Up GPU connectivity.

All are looking for IEEE 802.3 to define the Ethernet Physical Layer Specifications

Looking Closer at the Backend Network



Based on AI Datacenters and their Diverse Network Requirements, Ram Huggahalli (Microsoft), Ethernet Alliance TEF 2024, Oct 2024.

Why Now?

- 400 Gbps/lane development is already underway, but no IEEE 802.3 standard exists, creating urgency to align industry investment and avoid fragmentation
- AI network architectures require 400 Gbps/lane to enable high-radix systems — demand is immediate and growing
- Standardization now ensures multi-vendor interoperability and leverages Ethernet's broad ecosystem for faster, lower-cost deployment of next-generation technologies

Logistics

- A consensus building presentation will be given during the IEEE 802.3 March 2026 Plenary meeting:
  - Tuesday, 10 March 2026 18:30-1945 PDT (UTC-7)
  - Details on IEEE 802.3 call and meeting calendar and IEEE 802 Plenary schedule
- The vote to determine whether a Study Group will be formed will take place at the IEEE 802.3 WG Closing Plenary on the afternoon of Thursday, 12 March 2026
- I would be happy to speak with anybody (in person or remote; please contact me at kent.lusted@synopsys.com for remote) to address questions or concerns
- I would be happy to add anybody who wishes to be listed as a supporter
  - You must ask to be a supporter before the motion to form the Study Group is considered

Supporters (1/2)

- Osorio, Luz - Nokia
- Ghiasi, Ali - Ghiasi Quantum, Marvell
- Ofelt, Dave - HPE
- Choudhury, Mabud - Genuine Optics
- El-Chayeb, Ahmad - Keysight Technologies
- Nicholl, Gary - Cisco
- Zimmerman, George - CME Consulting/Cisco, Eliyan
- Mascitto, Marco - Nokia
- Galan, Jose - Maxlinear
- Stephens, Jeremy - AMD
- Weaver, Jim - Arista
- Goergen, Joel - Cisco
- D'Ambrosia, John - FutureWei, US subsdiary of Huawei
- Calvin, John - Keysight Technologies
- Moorwood, Andy - Keysight Technologies
- Rabinovich, Rick - Keysight Technologies
- Sun, Junqing (Phil) - Credo
- Ramesh, Sridhar - Maxlinear
- Estes, Dave - Viavi
- Brooks, Paul - Viavi
- Nakamoto, Ed - Viavi
- Lewis, Jon - Dell Technologies
- Stone, Rob - Meta
- Zhang, Geoff - AMD
- Li, Tobey - MediaTek
- Wu, Mau-Lin - MediaTek
- Nicholl, Shawn - AMD
- Klempa, Michael - Qualcomm
- Brown, Matt - Qualcomm
- Vidal, Or - Qualcomm
- Bowman, Kurtis - AMD/UALink
- Akinwale, Femi - Intel
- Johnson, John - Broadcom
- Parthasarathy, Vasudevan - Broadcom
- Muth, Karl - Broadcom
- Liu, Cathy - Broadcom
- Mellitz, Rich - Samtec
- Gore, Brandon - Samtec
- Cirit, Halil - Meta
- Opsasnick , Eugene - Broadcom
- Simms, Bill - nvidia
- Tooyserkani, Pirooz - Cisco
- Kabra, Lokesh - Synopsys
- Bhatt, Vipul - Coherent
- Cole, Chris - Coherent
- Rodes, Roberto - Coherent
- Biederman, Dan - Eridu AI
- Patra, Lenin - Marvell
- Kochuparambil, Beth - Cisco
- Tang, Yi - Cisco
- Noujeim, Leesa - Google
- Kareti, Upen Reddy - Cisco
- Ben-Artsi, Liav - Marvell
- Williams, Tom - Cisco
- Welch, Brian - Cisco
- Dudek, Mike - Marvell
- Kimber, Mark - Semtech
- Ran, Adee - Cisco
- Kutscher, Noam - Marvell
- He, Xiang - Huawei
- Mi, Guangcan - Huawei
- Sommers, Scott - Molex

Supporters (2/2)

- Marshall, John - AMD
- Li, Mike - AMD
- Issenhuth, Tom - Huawei
- Chen, David CC - AOI
- Tracy, Nathan - TE
- Heck, Howard - TE
- Huggahalli, Ram - Microsoft
- Maniloff, Eric - Ciena
- Wingrove, Mike - Ciena
- Yu, Rangchen Ryan - Terahop
- Huber, Tom - Nokia
- Bruckman, Leon - nvidia
- Marques, Flavio - Lightera
- Palkert, Tom - Samtec
- Wang, Sharon - TE Connectivity
- Parsons, Earl - CommScope Amphenol
- He, Michael - Terahop
- Pepper, Jerry - Keysight
- Bernier, Eric - Huawei
- Slavick, Jeff - Broadcom
- Kocsis, Sam - Amphenol
- D'Silva, Hansel - Amphenol
- Shakiba, Hossein - Huawei
- Jackson, Kenneth - Sumitomo
- Zivny, Pavel - Multilane
- Muhigana, Ernest - Macom
- Landry, Gary - Texas Instruments
- Tartaglia, Antonio - Ericsson
- Parkholm, Ulf - Ericsson
- Lessard, Stephane - Ericsson
- Chan, Jason - Arista
- Yu, Xu Helen - Huawei
- Healey, Adam – Broadcom

Call For Interest

With the rapid adoption of Artificial Intelligence (AI) tools and technology, there is a desire to use Ethernet in high-bandwidth, high-growth AI cluster networks, as well as traditional front-end networks for server and switch attachment. The Ethernet community must quickly respond to support the AI network time-to-market requirements and use cases. A number of technology improvements should be investigated to increase the per-lane signaling rate of electrical and optical Ethernet interconnects for the radix-optimized connectivity essential for communication between the high-performance compute devices and intermediate network switch devices.

This call for interest is to initiate a Study Group to develop a Project Authorization Request (PAR) and Criteria for Standards Development (CSD) for Physical Layer specifications supporting existing Ethernet rates using 400 Gbps-per-lane signaling for electrical interconnects as well as optical interconnects with reaches of up to 500 meters.

https://ieee802.org/3/cfi/request_0326_1.html

Questions?

THANK YOU!