

IEEE 802.3
Interpretations Report

November 13th, 2003
Albuquerque, NM
David Law

Activities this week

- Met Wednesday afternoon
- 5 Interpretations considered
 - 1-11/03 - Conformance Test signal at TP3 for receiver testing (38.6.11)
 - 2-11/03 - DTE Power via MDI Isolation (33.4.1)
 - 3-11/03 - Isolation requirements (14.3.1.1)
 - 4-11/03 - Isolation requirements (14.3.1.1)
 - 5-11/03 - 10GBASE-X check_end function (48.2.6.1.4)

Interpretation Number: 1-11/03
Topic: Conformance Test signal at TP3
for receiver testing
Relevant Clause: 38.6.11
Classification:

Interpretation Request

In the IEEE Std 802.3 2000 as well as 2002, in Section 38.6.11 "Conformance Test signal at TP3 for receiver testing", a 4th order BT filter is specified in the text and in Figure 38-5. We are in the process of building this test system and the vendors we are working with have stated that not enough information has been provided. Specifically, they have said that the BT coefficient of this filter needs to be specified. Can you provide this information to me? Also, a change to the standard may be in order to include this information.

38.6.11 Conformance test signal at TP3 for receiver testing

Figure 38–5 shows the recommended test set up for producing the conformance test signal at TP3. The coaxial cable is adjusted in length to produce the correct DCD component of DJ. Since the coaxial cable can produce the incorrect ISI, a limiting amplifier is used to restore fast rise and fall times. A Bessel-Thomson filter is selected to produce the minimum ISI induced eye closure as specified per Table 38–4 for 1000BASE-SX and Table 38–8 for 1000BASE-LX. This conditioned signal is used to drive a high bandwidth linearly modulated laser source.

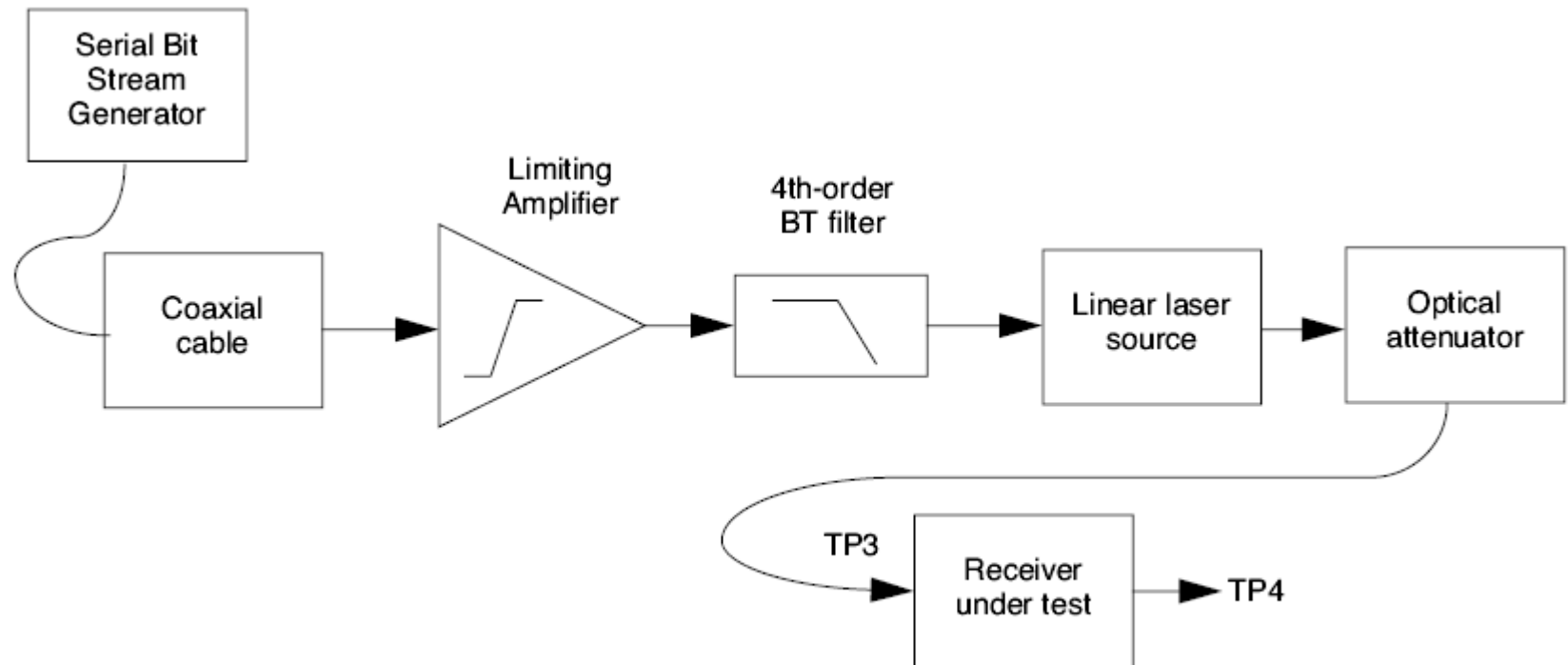


Figure 38–5—Apparatus for generating receiver conformance test signal at TP3

Interpretation Number: 1-11/03
Topic: Conformance Test signal at TP3
for receiver testing
Relevant Clause: 38.6.11
Classification: Unambiguous

Interpretation for IEEE Std 802.3-2002

The standard states in the penultimate paragraph of subclause 38.6.5 that 'A Bessel-Thomson filter is selected to produce the minimum ISI induced eye closure as specified per Table 38-4 for 1000BASE-SX and Table 38-8 for 1000BASE-LX.'

The functional test blocks, including the Bessel-Thomson filter, are intentionally not specified in detail in order to provide maximum flexibility in implementation.

What is specified instead is the behavior required. It is therefore essential that in a real world design without ideal components, the filter response be the response of the assembly of selected components used to implement the function.

The burden is therefore left on the implementer to select the filter such that the behavior, in conjunction with other real world components selected by the implementer, meets the requirements of the specification, specifically in the case of the filter '... the minimum ISI induced eye closure as specified per Table 38-4 for 1000BASE-SX and Table 38-8 for 1000BASE-LX.'

We believe that specification of the test set up is fully specified.

Interpretation Number: 2-11/03 – Item 1
Topic: DTE Power via MDI Isolation
Relevant Clause: 33.2.6.1
Classification:

Interpretation Request

Clause 33.2.6.1 Detection Criteria

The following is a note in this clause:

NOTE – Caution, in a multiport system, the implementer should maintain DC isolation through the termination circuitry to eliminate cross-port leakage currents.

This may be interpreted to mean that the implementer has the choice to prevent leakage or not prevent leakage port-to-port in a multiport PSE. The word ‘shall’ is not used.

How is this to be interpreted considering the clauses below?

Clause 33.4.1 Isolation

33.2.6.1 Detection criteria

A PSE shall accept as a valid signature a link section with both of the following characteristics between the powering pairs with an offset voltage up to V_{os} max and an offset current up to I_{os} max, as specified in Table 33–2:

- a) Signature resistance R_{good} , and
- b) Parallel signature capacitance C_{good} .

NOTE—Caution, in a multiport system, the implementer should maintain DC isolation through the termination circuitry to eliminate cross-port leakage currents.

Interpretation Number: 2-11/03 – Item 1
Topic: DTE Power via MDI Isolation
Relevant Clause: 33.2.6.1
Classification: Unambiguous

Interpretation for IEEE std 802.3-2002

The text referenced is contained in a note, it is therefore not a mandatory requirement.

Since the note is attached to Subclause 33.2.6.1 'Detection criteria', which specifies the behavioral requirements of the PD detection function in a PSE, it is this function the note is addressing. As the note states, it relates to DC isolation for termination circuitry in a multi-port system. The note is advising the implementer to eliminate cross port leakage current as this may interfere with the detection function specified in this subclause.

The scope of a note is limited to the clause or subclause to which it is attached.

Interpretation Number: 2-11/03 – Item 2
Topic: DTE Power via MDI Isolation
Relevant Clause: 33.4.1
Classification:

Clause 33.4.1 Isolation

Text in this clause is as follows:

Conductive link segments that have different isolation and grounding requirements shall have those requirements provided by port-to-port isolation of network interface devices (NIDS).

There are two implications here:

One, there exists port-to-port isolation in multiport NIDS as the isolation provides for different grounding and isolation requirements. Is there a requirement for port-to-port isolation in multi-port NIDS?

Two, link segments that have the same isolation and grounding requirements are not covered by this port-to-port isolation...or are they?

There seems to be a requirement for port-to-port isolation, i.e., the presence of ports with different or the same isolation requirements, does not remove the requirement for port-to-port isolation.

How is this to be interpreted considering Clause 33.2.6.1 and Clause 33.4.1.1.1?

33.4.1 Isolation

The PSE shall provide electrical isolation between the PI device circuits, including frame ground (if any), and all PI leads.

The PD shall provide electrical isolation between all external conductors, including frame ground (if any), and all PI leads.

This electrical isolation shall be in accordance with the isolation requirements between SELV circuits and telecommunication network connections in subclause 6.2 of IEC 60950-1:2001.

This electrical isolation shall withstand at least one of the following electrical strength tests:

- a) 1500 V_{rms} steady-state at 50-60 Hz for 60 seconds, applied as specified in subclause 6.2 of IEC 60950-1:2001.
- b) An impulse test consisting of a 1500 V, 10/700 μ s waveform, applied 10 times, with a 60 second interval between pulses, applied as specified in subclause 6.2 of IEC 60950-1:2001.

There shall be no insulation breakdown, as defined in subclause 6.2.2.3 of IEC 60950-1:2001.

Conductive link segments that have different isolation and grounding requirements shall have those requirements provided by the port-to-port isolation of network interface devices (NID).

Interpretation Number: 2-11/03 – Item 2
Topic: DTE Power via MDI Isolation
Relevant Clause: 33.4.1
Classification: Unambiguous

Interpretation for IEEE std 802.3-2002

The standard states in the first paragraph of 33.4.1 that 'The PSE shall provide electrical isolation between the PI device circuits, including frame ground (if any), and all PI leads.'. This does not place any requirement for isolation between PI leads on differing ports on a multiport device. The 8th paragraph quoted in the request relates to the case of different isolation and grounding requirements on the link segments attached to the ports, such as where there are differing mains supplies. In the case where this does not exist this requirement does not need to be met.

It should be noted that there is a requirement that all equipment that meets this standard meets the safety requirements specified in subclause 33.5.1 'General safety'.

Interpretation Number: 2-11/03 – Item 3
Topic: DTE Power via MDI Isolation
Relevant Clause: 33.4.1.1.1
Classification: Ambiguous

Clause 33.4.1.1 Electrical Isolation Environments

The Environment A definition text is as follows:

Environment A – When a LAN or LAN segment, with all its associated interconnected equipment, is entirely contained within a single low-voltage power distribution system and within a single building.

What is the definition of ‘single low-voltage power distribution’?

Interpretation for IEEE std 802.3-2002

This represents an ambiguity within the standard. This issue is being referred to the maintenance process for possible action.

Interpretation Number: 2-11/03 – Item 4
Topic: DTE Power via MDI Isolation
Relevant Clause: 33.4.1.1.1
Classification:

Clause 33.4.1.1.1 – Environment A requirements

The first statement of the clause requires the following:

Attachment of network segments via network interface devices (NIDS) that have multiple instances of a twisted pair MDI requires electrical isolation between each segment and the protective ground of the NID.

There is an implication that each segment need not be isolated from the other segments (port-to-port isolation) in a multiport NID, but all isolated from protective ground.

How is this statement to be interpreted considering Clause 33.2.6.1 and Clause 33.4.1?

Also, the following text is located in this clause:

A multi-port NID complying with Environment A requirements does not require electrical power isolation between link segments.

This appears to be a circular reference since the above requirement is referencing the requirement clause in which the text itself is located. How is this to be interpreted?

Also, how is this statement to be interpreted considering Clause 33.2.6.1 and Clause 33.4.1?

33.4.1.1.1 Environment A requirements

Attachment of network segments via NIDs that have multiple instances of a twisted pair MDI requires electrical isolation between each segment and the protective ground of the NID.

For NIDs, the requirement for isolation is encompassed within the isolation requirements of the basic MAU/PHY/medium standard. (See 14.3.1.1, TP-PMD, and 40.6.1.1.) Equipment with multiple instances of PSE and/or PD shall meet or exceed the isolation requirement of the MAU/PHY with which they are associated.

A multi-port NID complying with Environment A requirements does not require electrical power isolation between link segments.

An Environment A PSE shall switch the more negative conductor. It is allowable to switch both conductors.

Interpretation Number:	2-11/03 – Item 4
Topic:	DTE Power via MDI Isolation
Relevant Clause:	33.4.1.1.1
Classification:	Unambiguous

Interpretation for IEEE std 802.3-2002

The standard states in the first paragraph of subclause of 33.4.1.1.1 that isolation is required between MDI and protective ground of the NID, there is no requirement stated here for isolation between MDIs.

Interpretation Number: 3-11/03
Topic: Isolation requirements
Relevant Clause: 14.3.1.1
Classification:

Interpretation Request

I would like to request an interpretation for IEEE802.3 2002 specs (clause 14.3.1.1 Isolation Requirement) which should be the same as IEEE802.3 1998 or 2000.

This clause says: "The MAU shall provide isolation between the DTE physical layer circuits including frame ground and all MDI leads including those not used by 10Base-T. This electrical separation shall withstand at least one of the following electrical strength tests"

Now, we use gang RJ45 connectors in our designs which have integrated LEDs for status indication. Those LEDs are driven by the DTE physical layer circuit.

Our interpretation to the above clause is that those LED leads on the the RJ45 connector need to be isolated from MDI leads by 2250Vdc or 1.5KVrm or the pulse test. So, we basically believe that LED leads are part of DTE physical layer circuit. However, when we talk to the vendor they think that they only need to isolate MDI leads from the frame ground and isolation of LED leads to MDI leads is not a requirement by the standard.

If we follow this clause further, we find that it directs to IEC60950 and therefore we think LED leads and MDI leads should have a minimum clearance of 60mil per Annex G of IEC60950.

14.2.1.7 Link Integrity Test function requirements

If a visible indicator is provided on the MAU to indicate the link status, it is recommended that the color be green and that the indicator be labeled appropriately. It is further recommended that the indicator be on when the MAU is in the Link Test Pass state and off otherwise.

Interpretation Number:	3-11/03
Topic:	Isolation requirements
Relevant Clause:	14.3.1.1
Classification:	Beyond the scope of the Standard

Interpretation for IEEE std 802.3-2002

The implementation details of the 'visible indicator' recommended in subclause 14.2.1.7 'Link Integrity Test function requirements' is beyond the scope of the Standard. This request is therefore being returned to you because it does not constitute a request for interpretation but rather a request for consultation advice.

Interpretation Number:	4-11/03
Topic:	Isolation requirements
Relevant Clause:	14.3.1.1
Classification:	Substantially identical to existing interpretation

Interpretation Request

A customer has raised a question regarding the 802.3 2002 specification and our modular jack connector which is shielded and has LEDs. Our customer is testing our connector per section '14.3.1.1 Isolation Requirement' and believe that the electrical isolation requirement applies to the following:

- 1.) Signal leads to ground (our shield)
- 2.) LED leads to ground (our shield)
- 3.) LED leads to signal leads

When we designed the modular jack in question, our interpretation of the 802.3 specification was that electrical isolation was required only between signal leads and ground and in no manner does the 802.3 spec dictate electrical isolation between LED/ground nor LED/signal. We would like to know IEEE's interpretation of the electrical isolation requirement in this matter.

Interpretation for IEEE std 802.3-2002

This request is substantially identical to interpretation 3-11/03, and the resolution of that interpretation applies in this case.

Interpretation Number: 5-11/03
Topic: 10GBASE-X check_end function
Relevant Clause: 48.2.6.1.4
Classification:

Interpretation Request

Clause 48.2.6.1.4 of IEEE Std. 802.3ae-2002 defines the check_end function. The definition of this function is given here:

Prescient Terminate function used by the PCS Receive process to set the RXD<31:0> and RXC<3:0> signals to indicate Error if a running disparity error was propagated to any Idle code-groups in ||T||, or to the column following ||T||. The XGMII Error control character is returned in all lanes less than n in ||T||, where n identifies the specific Terminate ordered-set ||Tn||, for which a running disparity error or any code-groups other than /A/or /K/are recognized in the column following ||T||. The XGMII Error control character is also returned in all lanes greater than n in the column prior to ||T||, where n identifies the specific Terminate ordered-set ||T n ||, for which a running disparity error or any code group other than /K/is recognized in the corresponding lane of ||T||. For all other lanes the value set previously is retained.

The first sentence clearly states that the purpose of this function is to catch errors that have propagated into idle code-groups either in ||T|| or in the column following ||T||. This also implies that the function does not intend to catch errors that could not possibly have propagated into the idle code-groups. There is no additional information in this sentence, and it is largely a description of the function.

The second sentence is: "The XGMII Error control character is returned in all lanes less than n in ||T||, where n identifies the specific Terminate ordered-set ||Tn||, for which a running disparity error or any code-groups other than /A/ or /K/ are recognized in the column following ||T||."

It is not clear from this sentence what the desired behavior should be. Please examine the following example with the /T/ contained in lane 2. In this example, * refers to a running disparity error or code-group other than /A/ or /K/. There are four cases shown in this example, each with the error occurring in a different lane. Each of the options listed below corresponds to the XGMII data after being received by the PCS.

For the second sentence of the check_end function, there are two interpretations over which frames get discarded, and two interpretations on which code-groups are changed to /E/. It is not clear from the reading of the function which interpretations are correct.

Input of PCS receiver

Case 1	Case 2	Case 3	Case 4
0 1 2 3	0 1 2 3	0 1 2 3	0 1 2 3
D D D D	D D D D	D D D D	D D D D
D D T K	D D T K	D D T K	D D T K
* K K K	K * K K	K K * K	K K K *

In the first option, the error control character is returned for each instance; therefore assuring that the frames will not be accepted. No matter which lane has the error, the error control character will be returned in all lanes less than n .

Option 1

```

-----
0 1 2 3    0 1 2 3    0 1 2 3    0 1 2 3
D D D D    D D D D    D D D D    D D D D
E E T K    E E T K    E E T K    E E T K
E K K K    K E K K    K K E K    K K K E

```

In the second option, the error control character is only pushed back into the frame when the error occurs on a lane less than n . When the error occurs in lanes 2 or 3, it is not necessary to push the error back since these errors could not have been propagated through the frame. This allows the frames to be accepted when the error occurs in lanes 2 or 3. Also in this option, when the error is pushed back into the frame, all lanes less than n receive the error control character.

Option 2

```

-----
0 1 2 3    0 1 2 3    0 1 2 3    0 1 2 3
D D D D    D D D D    D D D D    D D D D
E E T K    E E T K    D D T K    D D T K
E K K K    K E K K    K K E K    K K K E

```

In the third option, the error control character is only pushed back into the frame when the error occurs on a lane less than n . In this option, the error control character is only returned in those lanes, which actually had the error, and not in any other lanes.

Option 3

```

-----
0 1 2 3    0 1 2 3    0 1 2 3    0 1 2 3
D D D D    D D D D    D D D D    D D D D
E D T K    D E T K    D D T K    D D T K
E K K K    K E K K    K K E K    K K K E

```

Which of the above interpretations (1, 2, or 3) is correct?

The original intent of the check_end function was that potentially valid frames not be invalidated by the PCS. When an error occurs in a column directly following a valid /T/, /K/, or /A/ codegroup, then the error could not have propagated through data code-groups in the frame, as the /T/, /K/, and /A/ code-groups will effectively prevent errors such as running disparity errors from going through them. Since the error could not possibly have occurred within the data portion of the frame, there should be no need for the PCS to invalidate the frame. One possible interpretation of the current text is that such action should be taken by the PCS.

It is not clear what the original intent of the `check_end` function was with respect to replacing data code-groups with error code-groups. The replacement of a single data code-group with an error code-group is sufficient to force the frame to be discarded. Also, since the lanes are independent of each other, it is not possible for an error to propagate from one lane to another. Although the insertion of multiple error code-groups will have the same result as the insertion of a single error code-group, it is possible that certain error counters may be caused to increment needlessly.

A survey of 4 different vendors showed at least 3 different interpretations of the `check_end` function. One vendor follows option 1 and discards frames that are otherwise valid. A different vendor follows option 2 and allows those frames to be received. A third and fourth vendor have implemented yet another interpretation, one that allows frames which should be discarded to be accepted. It seems clear that the current wording of the `check_end` function appears to be overly complicated and is easily given to misunderstanding and misinterpretation. Based on the outcome of this request, we are prepared to submit a maintenance request to clarify the wording of the function so that future implementations may benefit.

Case 1	Case 2	Case 3	Case 4
0 1 2 3	0 1 2 3	0 1 2 3	0 1 2 3
D D D D	D D D D	D D D D	D D D D
D D T K	D D T K	D D T K	D D T K
* K K K	K * K K	K K * K	K K K *

Option 1

0 1 2 3	0 1 2 3	0 1 2 3	0 1 2 3
D D D D	D D D D	D D D D	D D D D
E E T K	E E T K	E E T K	E E T K
E K K K	K E K K	K K E K	K K K E

Option 2

0 1 2 3	0 1 2 3	0 1 2 3	0 1 2 3
D D D D	D D D D	D D D D	D D D D
E E T K	E E T K	D D T K	D D T K
E K K K	K E K K	K K E K	K K K E

Option 3

0 1 2 3	0 1 2 3	0 1 2 3	0 1 2 3
D D D D	D D D D	D D D D	D D D D
E D T K	D E T K	D D T K	D D T K
E K K K	K E K K	K K E K	K K K E

Classification:

Unambiguous

Interpretation for IEEE std 802.3-2002

The standard states in subclause 48.2.6.1.4 that 'The XGMII Error control character is returned in all lanes less than n in $||T||$, where n identifies the specific Terminate ordered-set $||T_n||$, for which a running disparity error or any code-groups other than /A/or /K/are recognized in the column following $||T||$. The XGMII Error control character is also returned in all lanes greater than n in the column prior to $||T||$, where n identifies the specific Terminate ordered-set $||T_n||$, for which a running disparity error or any code group other than /K/is recognized in the corresponding lane of $||T||$. For all other lanes the value set previously is retained.'

The correct option is therefore 3.

In Cases 1 to 4 of the 'Input to PCS receiver' shown in the request, $n=2$ as the /T/ appears in lane 2. Therefore all lanes less than n in these examples means lanes 0 and 1.

In 'Case 1' shown an error appears in lane 0 which meets the condition of an error in lane less than n . Therefore an error is inserted in the $||T||$ for lane 0 because it meets the condition of a disparity error in a lane less than n with a running disparity error in the following column. No error is inserted in lane 1 because there is no error in the following column.

In case 3 an error appears in lane 2 which does not meet the condition of an error in lane less than n . No errors are inserted.

IEEE 802.3 Motion

IEEE 802.3 approves the proposed Interpretation responses to the Interpretation requests 1-11/03 through 5-11/03 as presented without the need for a 30 day letter ballot.

M: David Law

S: Steve Carlson Tech 75%/Proc ~~50%~~

PASSED/~~FAILED~~

Date:

Y: 23

N: 0

A: 2

Time: