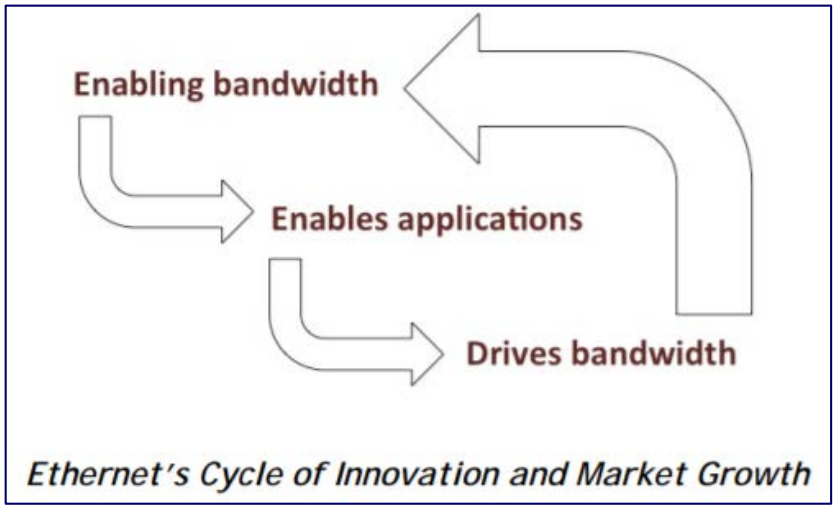
IEEE 802.3 Call-for-Interest Opening Report

100 Gb/s per Lane for Electrical Interfaces and PHYs

Motivation for 100 Gb/s per Lane

With next steps in Ethernet, comes the needed next step in interfaces.

- Faceplate density
- Chip breakout
- System throughput

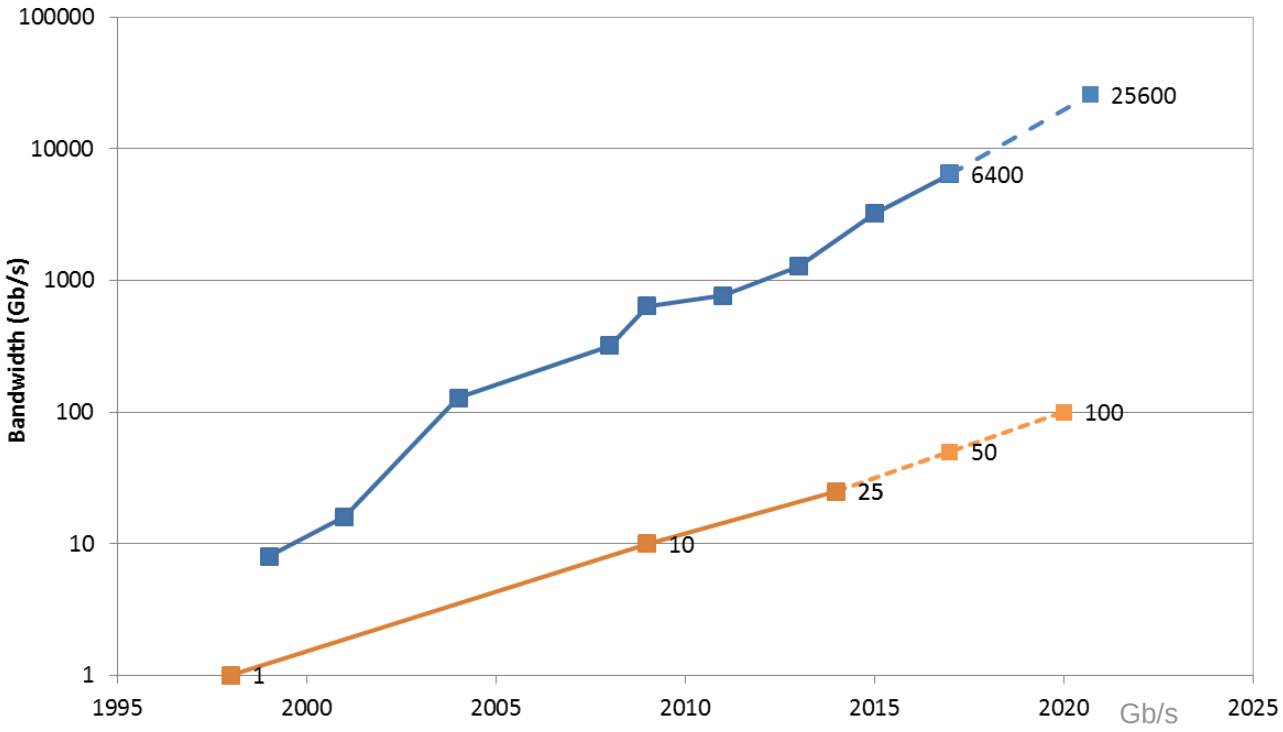


Ethernet's Cycle of Innovation and Market Growth

They are all tied together!

*Web-scale data centers and cloud based service are presented as leading applications

Need to support I/O Bandwidth demands



- Single ASIC I/O capacity is doubling every ~2 years
- 100G/lane is the next logical step
- We need to study and frame the 100G/lane discussion NOW so the industry can plan

Logistics

There will be a consensus building presentation:

- Tuesday, November 7th @ 7:30-8:25pm
- Room TBA

CFI Consensus Presentation-

http://www.ieee802.org/3/cfi/request_1117_3.html

Call-for-Interest

The continual growth of bandwidth demand has driven evolution of higher Ethernet speeds, most recently with 100 Gb/s, 200 Gb/s, and 400 Gb/s Ethernet, as demonstrated by related 802.3 projects over the past 5 years. Ongoing advancement in SERDES technology to higher rates of operation will enable the opportunity to develop improved interfaces for AUIs, backplanes, and cables at these rates. This call for interest is to assess support for the formation of an 802.3 study group to explore the uses and development of electrical interfaces and electrical PHYs using 100Gb/s per lane technology.