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Title:	Impact on timing performance due to Ethernet PHY

LIAISON STATEMENT

For action to:	IEEE 802.3
For comment to:	
For information to:	IEEE 1588
Approval:	ITU-T SG15 Q13/15 (Rapporteur meeting, Auckland, 9-13 October 2017)
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Keywords:	Time synchronization, PHY, IEEE802.3
Abstract:	Liaison to IEEE802.1 concerning the impact on timing performance due to Ethernet PHY

Within ITU-T SG15, Q13 is responsible for Network synchronization and time distribution performance.

Over the last years Q13 has developed various Recommendations addressing requirements and solutions for the distribution of frequency synchronization and time synchronization over Telecommunications networks, addressing the needs of various applications (e.g. radio base stations). Among these Recommendations, ITU-T G.8271 (ref.1), Time and phase synchronization aspects of telecommunications networks, provides some high-level requirements and guidelines as related to the distribution of accurate time synchronization over telecommunication networks, with particular focus on packet networks and OTN networks.

Distribution of time synchronization via two-way timing protocols such as PTP, Precision Time Protocol (ref. 4) is significantly impacted by any source of asymmetric delay between the two transmission directions.

ITU-T G.8271 provides some information on potential sources of timing errors and delay asymmetries (see Appendix I, III, IV, V).

In particular, as indicated in Appendix I.7.2, an important source of error as related to the (hardware) timestamping of incoming/outgoing timing packets, may be in the PHY. Some of the hardware-timestamping related noise depends on the specific interface used and on the implementation of the related PHY components.

Relevant text from G.8271 is copied below:

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I.7.2   PHY latency variation and asymmetry

This noise source is related to the hardware timestamping function, i.e., to the difference between the timestamp measurement point and the interface to the medium (e.g., 802.3bf defines the minimum and maximum transmit and receive values possible for each PHY supporting 802.3bf). For a proper implementation, this will typically be in the range of nanoseconds. The PHY latency asymmetry is defined as $(d_{tx}–d_{rx})/2$, where d_{tx} is the delay on the transmit path and d_{rx} is the delay on the receive path, as indicated in clause I.6 and Figure I.1.

This noise source is applicable to the packet master clock function (in a T-GM or a T-BC) and packet slave clock function (in a T-BC or in a T-TSC).

The way the noise source, e_{phy}, is modelled is for further study.

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With the intention to address end-to-end time synchronization requirements significantly better than 1.5 μs, e.g., to address potential new requirements that may be required for some 5G related functions it is important that phase error introduced by the PHY components is well controlled, possibly, according to strict standard rules, to within a few ns. This is particularly critical for both static time error types and noise sources with low frequency components (i.e. that would be difficult to filter out).

At the Q13 meeting held in Auckland in October 2017, attention was brought to some specific sources of delay that may be generated in the PHY.

With reference to the IEEE802.3 25Gbps interface (ref. 2 and ref. 3) FEC may have to be implemented (see figure 108-1 in ref.2), and it could be a source of impairments during the PTP timestamping process.

In fact, FEC processing (see section 108 in ref. 2) implies operations such as RS-FEC encoding scheme and Codeword insertion. In this case, the encoding scheme involves 140 UI (about 5 nanoseconds) every RS-FEC frame and 257 UI (10 nanoseconds) every 1024 RS-FEC frame.

The understanding is that, depending on where timestamping is performed, and depending on the position of the PTP message in the RS-FEC frame, the PTP timestamping could be randomly impacted by a (variable) value up to 15 nanoseconds, which may not be acceptable for the support of some applications.

Rate compensation may be another potential source of impairments.

With reference to Figure108-1 in ref.2, performing the timestamping in transmission above the RS-FEC layer in both transmit and reception, may remove some of this noise.

Taking into account the delay added by the RS-FEC is another approach that could be considered (e.g.,. timestamping is done below the RS-FEC layer in both transmission and reception).

In any case, it is considered important that a consistent approach is followed among vendors in order to control the timestamping noise to values on the order of a few nanoseconds (e.g., a couple of nanoseconds).

Alignment Markers, in the case of multilane interfaces, is another potential source of variable delays that may result in timing impairments of frames carrying timing information.

Q13 would like to ask IEEE802.3 for advice concerning the specific aspects described in this liaison.

Q13 would also appreciate receiving any updates concerning actions that may have been taken in order to guarantee that delays added by the Ethernet PHY components are properly controlled to within a small uncertainty value (e.g., a couple of nanoseconds) and/or consider if any action would be required to be initiated.

We look forward to continuing our good working relationship with the IEEE 802.3 Working Group.

References

1. ITU-T Recc. G.8271, Time and phase synchronization aspects of telecommunications networks

2. IEEE Std 802.3by™-2016, Amendment to IEEE Std 802.3™-2015

3. IEEE P802.3cc™/D3.3, Draft Standard for Ethernet Amendment: Physical Layer and Management Parameters for Serial 25 Gb/s Ethernet Operation Over Single-Mode Fiber

4. IEEE 1588-2008, IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems

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