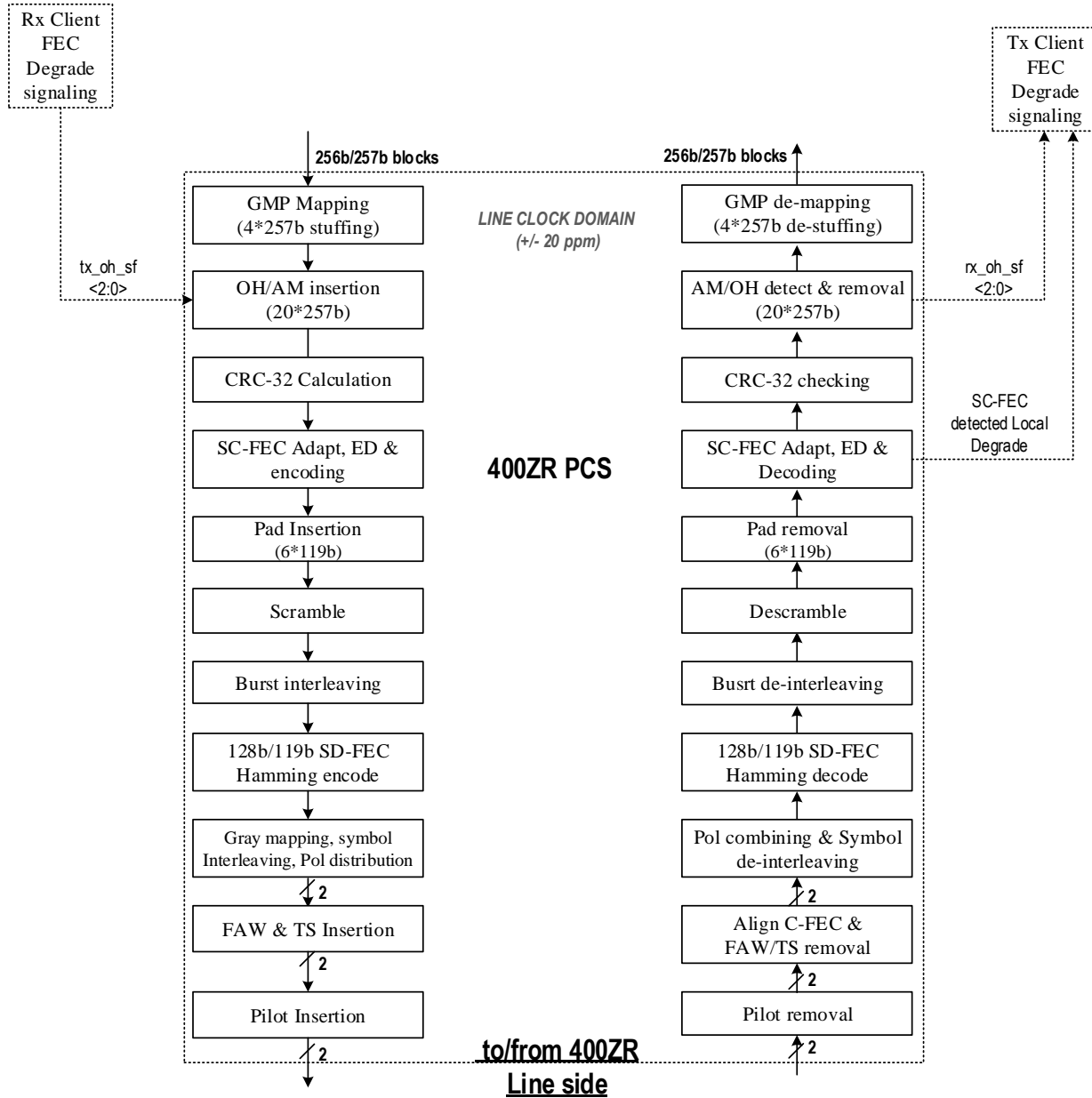


The Physical and Link Layer (PLL) Working Group also agreed on the operation and rate expansion of functional blocks completing the datapath to the 400ZR single carrier coherent channel interface. The complete datapath is shown below.



Key decisions made during this meeting included:

- Asynchronous mapping and rate adaptation of the 256b/257b encoded 400GE PCS signal to 400ZR frame using simplified GMP. Supports both frequency and Data transparency. Line side frequency tolerance is specified at +/-20ppm.
- Line side framing and pilot symbol insertion.
 - o A set of 181888 symbols (super-frame) aligned to 5 SC-FEC blocks, polarity interleaved to X-pol, Y-pol.
 - o Pilot symbols inserted after every block of 31 data symbols
 - o DSP sub-framing consisting of 3712 symbols.

The 400ZR line side interface is DP-16QAM operating at 59.84375 Gbaud.

This project will develop an implementation agreement (IA) targeted at (passive) single channel ZR and (amplified) short-reach DWDM /DCI pluggable modules with distances supported from 80-120 km.

We will continue to update the IEEE 802.3 Working Group on the progress on 400ZR IA. Our next meeting in San Antonio, TX, USA January 15th - 18th, 2018.

Sincerely,

A yellow rectangular box redacting the signature of Klaus-Holger Otto.

Klaus-Holger Otto,
OIF Technical Committee Chair (klaus-holger.otto@nokia.com)