IEEE 802.3 Ethernet Working Group
Liaison Communication

Source:	IEEE 802.3 Working Group[1]	
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From:	David Law	Chair, IEEE 802.3 Ethernet Working Group

Subject: Reply to Incoming Liaison 3N1299, demating under load

Approval: Agreed to at IEEE 802.3 plenary teleconference meeting, 18 November 2021

Dear Mr Oehler,

We would like to thank you for your communication 3N1299. The IEEE P802.3da 10 Mb/s Single Pair Multidrop Enhancements (SPMD) Task Force has reviewed the previously provided circuit diagrams and note that Power over Ethernet (PoE) uses a common mode powering technique while Single-pair Power over Ethernet (SPoE) employs a differential mode. Therefore, the circuit diagrams will be different between the two powering methods. Circuit diagrams for SPoE demating under load testing are attached. These diagrams are for the point-to-point case only.

[1] This document solely represents the views of the IEEE 802.3 Working Group and does not necessarily represent a position of the IEEE, the IEEE Standards Association, or IEEE 802.

At the current time, IEEE 802.3 does not specify powering on multidrop segments but is considering such a specification in the IEEE P802.3da Task Force. The IEEE 802.3 Working Group will inform SC25 when the test circuits for multidrop segments are available.

Thank you for your consideration.

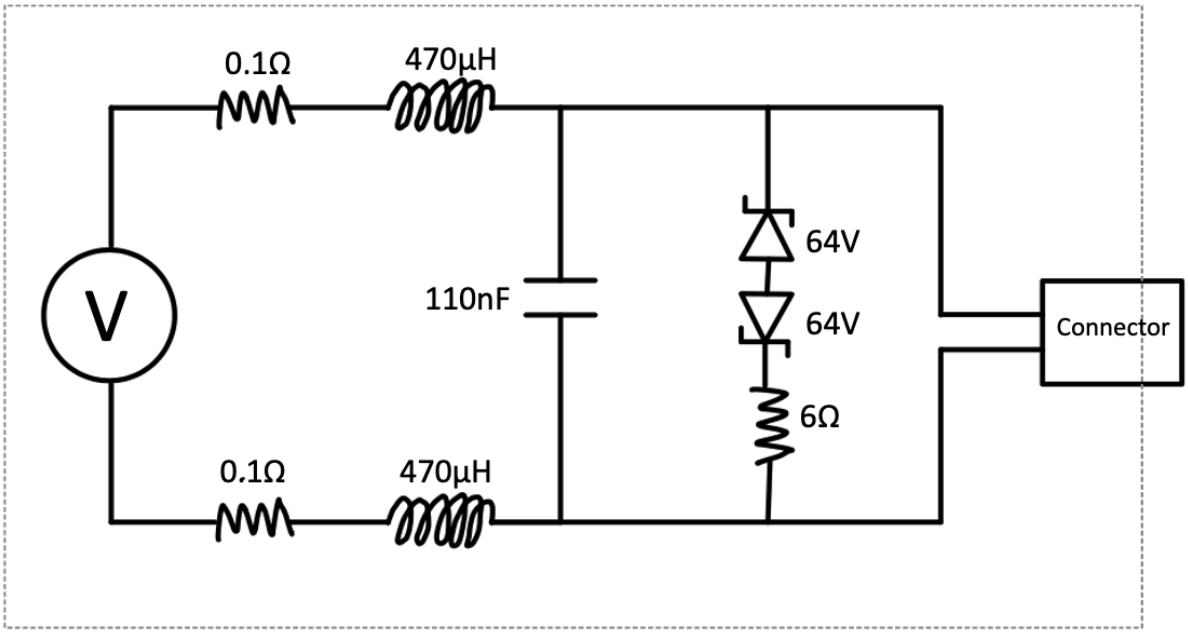
Sincerely,
David Law
Chair, IEEE 802.3 Ethernet Working Group

ATTACHMENT:

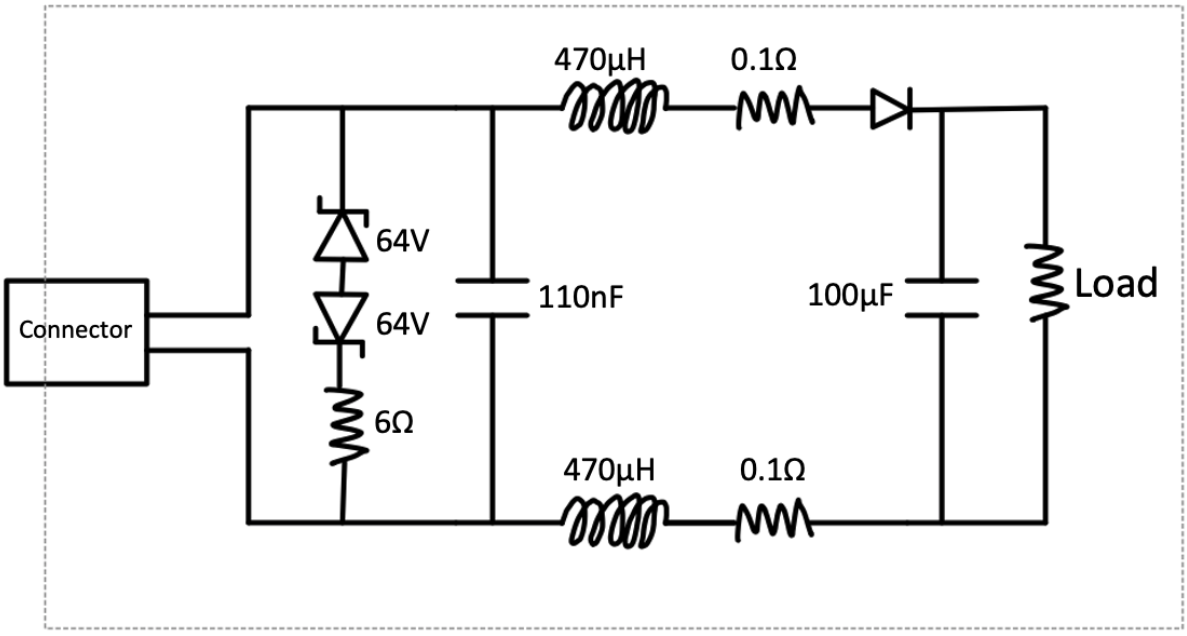
The goal of the test circuit is to generate a voltage and current that matches the maximum allowed by IEEE Std 802.3™-2018 as modified by the IEEE Std 802.3cg™-2019 standard with worst case expected circuit elements, based on the PoDL Class 15. To meet this goal, the system would have 50V and 1.579A at the test connector. Discussions of each element follows the circuit diagram.

Test Circuit Diagrams for PoDL unmating under load:

PSE MODEL



PD MODEL



Discussion of the elements:

The power supply: It is expected to be in the range of 51V to generate 50V at 1.579A at the test connector. Therefore, the test circuit will need an adjustable supply.

The inductors:

Inductance (@ 100 kHz, 0.1 Vrms, 0 Adc): 470 +/- 10% uH
DC resistance: 0.2 Ohms typical, 0.23 Ohms maximum
Self-resonant frequency: 1.35 MHz typical
Saturation current (@ 25C): 10% drop @ 2.4 A; 20% drop @ 2.7A; 30% drop @ 2.8A
Temperature rise: 20C rise @ 1.39A rms; 40C rise @ 2.10A rms

The TVS protection diodes: Actual systems will typically use smaller parts like the SM**A**J64A or SM**B**J64A. Since we expect that the tester will run MANY cycles, we recommend using an SM**D**J64A to prevent premature failure. In an attempt to match the performance of the smaller SMA or SMB parts, we've added an inline resistor in the range of 6 ohms. A standard value close to that is acceptable.

The PD load: This can be implemented with power resistors but is better achieved by a programmable load. This load has to dissipate as much as 80W, but the power dissipated in the PD coupling inductors, series resistors, and diode would need subtracted. A programable load in combination with a variable DC supply for the PSE will allow dialing in the proper source voltage and PD load to achieve the 50V, 1.579A target at the PSE.

An example of calculating voltage and load:

As stated, the DCR of the specified inductors is 0.2 ohms. Two 0.1 ohms resistors and two 0.2 ohms DCR inductors equals 0.6 ohms total. 0.6ohms * 1.579A = 0.94V. Set the power supply to 51V. Same 0.6 ohms in the PD also equaling a 1V drop, plus the diode, 1.7V yields 48.3V at the Load. 48.3V/1.579A = 30.6 ohms load at 77W. Set the programmable load to 30.6 ohms or 77W. Fine tune from there to get 50V and 1.579A at the test connector.