PoE Plus IEEE 802.3at Classification Ad Hoc

Resolving Draft 1.0 Comments in L1 Bucket

Clay Stanford
Linear Technology
December 5 and 12, 2007
Teleconference

C/ 33 SC 3.4.2 P 57 L 38 Stanford, Clay Linear Technology

Comment Type Comment Status D Ε

L1 adhoc

Define Mark Event Voltage range. It will make text more clear.

Define Reset Voltage range. It will make text more clear.

Label Reset Threshold Vreset_th to be more consistant.

SuggestedRemedy

Table 33-11a

Item 2: Add "10" to max column.

Item 5: Change Symbol from Vreset to Vreset_th

Add new item 6, Classification Reset Voltage Vreset V 0(V) 2.8(V) See 33.3.4.2.1

Proposed Response Response Status O

C/ 33 SC 3.4.2.1 P 57 L 53 Stanford, Clay Linear Technology

Comment Type Comment Status D

Text will be more clear if we use Vmark range.

SuggestedRemedy

Line 53 IS:

When the voltage at the PI is between VMark min and VMark_th min, a Type 2 PD shall return a non-valid detection signature as defined in Table 33-9.

Line 53 SHOULD BE:

When the voltage at the PI is IN THE RANGE OF Vmark, a Type 2 PD shall return a nonvalid detection signature as defined in Table 33-9.

Proposed Response

Response Status O

255 002

see 256

Table 33-11a-2-Event Physical Layer classification electrical requirements

Item	Parameter	Symbol	Units	Min	Max	Additional Information
1	Class Event Voltage	V _{Class}	V	14.5	20.5	
2	Mark Event Voltage	V_{Mark}	v	6.9	•	
3	Mark Event Current	I_{Mark}	mA	0.25	2	See 33.3.4.2.1
4	Mark Event Threshold	$V_{\mathrm{Mark_th}}$	v	10	14.5	See 33.3.4.2.1
5	Classification Reset Threshold	V_{Reset}	V	2.8	6.9	See 33.3.4.2.2

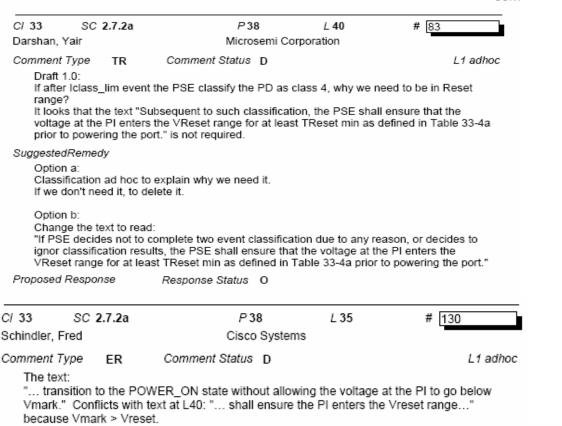
Vreset th

6 | Classification Reset Voltage | Vreset | V | 0 | 2.8 | See 33.3.4.2.1

Add this new entry

___ 10V

L1 adhoc



←-This comment is OBE. See 149 below. Sentence in question has been deleted.

←-This comment is OBE. See 149 below. Sentence in question has been deleted.

L 41

149

SuggestedRemedy
Have the L1 ad hoc provide text to correct this section.

Proposed Response Response Status O

R Comment Status A

defer to L1

If any measured IClass is equal to or greater than IClass_LIM min as defined in Table 33–4a, the PSE shall classify the PD as Class 04. If any measured IMark is greater than or equal to IMark_LIM min as defined in Table 33–4a, the PSE shall classify the PD as Class 0.

Subsequent to such classification, the PSE shall ensure that the voltage at the PI enters the VReset range for at least TReset min as definied in Table 33–4a prior to powering the port.

lclass is greater than Iclass_lim, the assigned class is Class4. There is no he voltage at the PI in this case. Whithout this sentence, if the 2-event classification succeeded, the PD will work correctly as class 4.

With a reset instead, the PD will work as a Type1 PD, wasting a lot of the allocated by the PSE.

SuggestedRemedy

Remove the sentence:

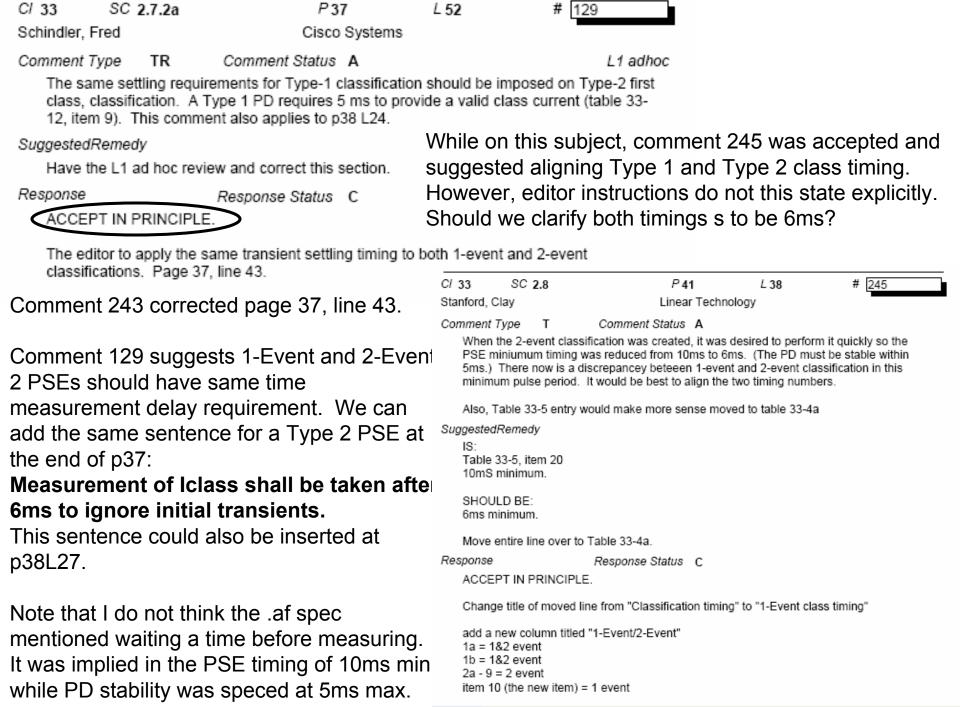
Subsequent to such classification, the PSE shall ensure that

the voltage at the PI enters the VReset range for at least TReset min as definied in Table 33–4a prior to powering the port.

Response

Response Status C

ACCEPT.



C/ 33 # 111 SC 3.4.2 P 57 L 50 Darshan, Yair Microsemi Corporation Comment Type Т Comment Status D L1 adhoc Draft 1.0: PD don't have to present class 4 for infinite classification attempts. Id adds thermal burden and costs. In any case if system has problems it may initiate consecutive startups every Ted which is defined in Table 33-5 item 21. SuggestedRemedy To be added after line 50. "PD may revert to IDLE state if PSE initiate more then 3 consecutive classification attempts within less then Ted as specified in Table 33-5." Proposed Response Response Status O defer to L1

A Type 2 PD shall return a Class 4 signature irrespective of the number of classification voltage probes performed by a PSE.

DISCUSS

Cl 33 SC 2.7.2a P38 L40 # 102

Darshan, Yair Microsemi Corporation

Comment Type TR Comment Status D L1 adhoc
Draft 1.0:

When PSE classify the PD after Iclas_LIM event it should get to Vreset for Treset prior to power the port.

In order to achieve this objective PD should consume some minimum current to allow PSE to reduce its port voltage due the capacitors in the channel.

SuggestedRemedy

The classification ad hoc to address this issue if it is possible to implement i.e. to have I>>0 at 2.8V to 6.9 Volt range for Treset.

Proposed Response Response Status O

defer to L1

DISCUSS

 C/ 33
 SC 2.7
 P 36
 L 27
 # 127

 Schindler, Fred
 Cisco Systems

 Comment Type
 TR
 Comment Status D
 L1 adhoc

The text:

"If a PSE successfully completes detection of a PD, but the PSE fails to complete classification of a PD, then a Type 1 PSE shall assign the PD to Class 0 and a Type 2 PSE shall assign the PD to class 4." imposes an unnecessary design requirement. This text also enables dump-Type 2 PDs that do not support DLL classification.

A system that does not provide a proper class is:

a) Experiencing a temporary fault that will rectify itself.

OR

b) Noncompliant.

A compliant Type-2 PD has not achieved mutual identification and will remain in type-1 power mode. Therefore, requiring class-4 power serves no legitimate purpose.

A PSE that classifies a PD and gets an invalid results is not probable because this occurs only when class current exceeds 51 mA.

SuggestedRemedy

Require PSEs that performs classification, to either repeat the detection and classification steps, or repeat the classification step, until legal responses are achieved.

Proposed Response Status O

defer to L1

DISCUSS

New Mark Timing Issue

PSE Mark Event timing

Table 33-4a, item 4 (D1.0, page 39, line 19)

- Though hardware will interoperate, port loading during event will effect observable timing behavior.
- Timing start and stop points are not clearly defined in standard.
- Intent was for timing event to commence when PSE starts driving port with Mark Event Voltage.
- Intent was for timing event to end when PSE stops driving port with Mark Event Voltage.
- Due to possibility of slow port discharge and lack of clear definition in standard, timing could be interpreted as occurring when port enters Mark Event Voltage range.

New Mark Timing Solution

TBD

New Turn On Delay Issue

- When Type 2 PDs is powered, it is powered up with Type 1 current and power limits.
- After power up, PSE transitions the power supply from Type 1 level to Type 2 level.
- The time when this occurs will depend on the classification type.
 - 2-Event classification will allow system to transition soon after power_on.
 - 1-Event + Layer 2 classification will take longer time period (1-2 minutes?) before the change is made.
- Finite time is required for PSE to make transition from low power to high power.
- PD must wait until PSE transition from low power to high power is complete before drawing higher current.
- This timing requirement is not currently specified in the standard.