Acheiving Maximum Power for PoE Plus

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Acknowledgements

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- Joe DeNicholas, National Semiconductor
- Hank Hinrichs, Pulse Engineering

Introduction

- Presentation Objectives
  - Show why ACB and BWD are needed
  - Show technical feasibility
  - Provide rough estimate of relative costs
- Acronyms and Abreviations
  - ACB = Active Current Balance
  - BWD = Broken-Wire Detection
  - 2P = 2-Pair wiring system
  - 4P = 4-Pair wiring system

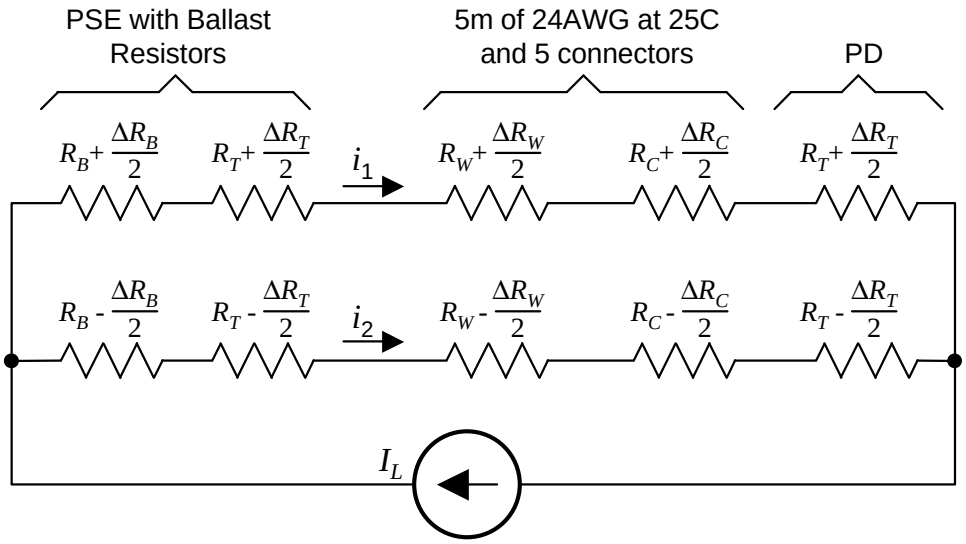
Assumptions

The following assumptions were used througout this document:

Assumption	Justification
The max current imbalance that can be tolerated is 8mA	Previous work done by Hinrichs and Ellsworth.
The max load current is 400mA per wire	Probably most extreme case.
4P wiring is used. 4P is not composed of two independant 2P systems.	This seems to be the most favored architecture at this time.

Why ACB is Needed

Transformer bias must be limited to approx 8mA, otherwise loss of inductance affects signal integrity.



Connectors: $R_C = 0$, $\Delta R_C = 0.05\Omega$ (Annex 33E)

Transformers: $R_T = 0.5\Omega$, $\Delta R_T = 0.03\Omega$ (Hienrichs)

WIre: $R_W = 0.42\Omega$ (5m), $\Delta R_W = 0.015 R_W$ (Annex 33E)

$$\frac{i_2 - i_1}{I_L} = \frac{\Delta R_B + 2\Delta R_T + \Delta R_W + \Delta R_C}{R_B + 2R_T + R_W + R_C} = \frac{\Delta R_B + 0.1163}{R_B + 1.42}$$

ANALYSIS

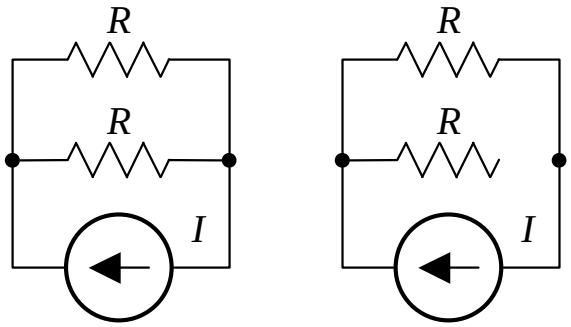
- Absolute worst case analysis of a single 24AWG pair with ballast resistors.
- Same method as 802.3af Annex 33E
- Transformer winding resistances added.
- Extended to 400mA per wire.
- Results verified with SPICE

RESULTS

- With no ballast (R_B=0), 8mA imbalance occurs when I_L=98mA. (This is why Annex 33E says you "must" have ballast resistors. Recommends 6.65Ω, 1%, 0.25W.)
- To acheive 8mA balance at I_L=800mA, the required ballast resistors are:
  - 20.5Ω, 0.5%, 3.5W or
  - 11.3Ω, 0.1%, 2W

Why BWD is Needed

2P Sytem: Power dissipation in a twisted pair doubles when one wire breaks.



$P_D = \frac{I^2R}{2}$ $P_D = I^2R$

4P Sytem: Assuming PD does not use separate converters.

No. of Broken Wires	Power Dissipation (relative to no broken wires)
1	133%
2	200%
3	400%

- Worst-case analysis becomes difficult in a 4P system: How many broken wires are a reasonable worst case?
- Can't use loss-of-link to detect breaks, because PD may not have Phy.

Summary: Acheiving Max Power

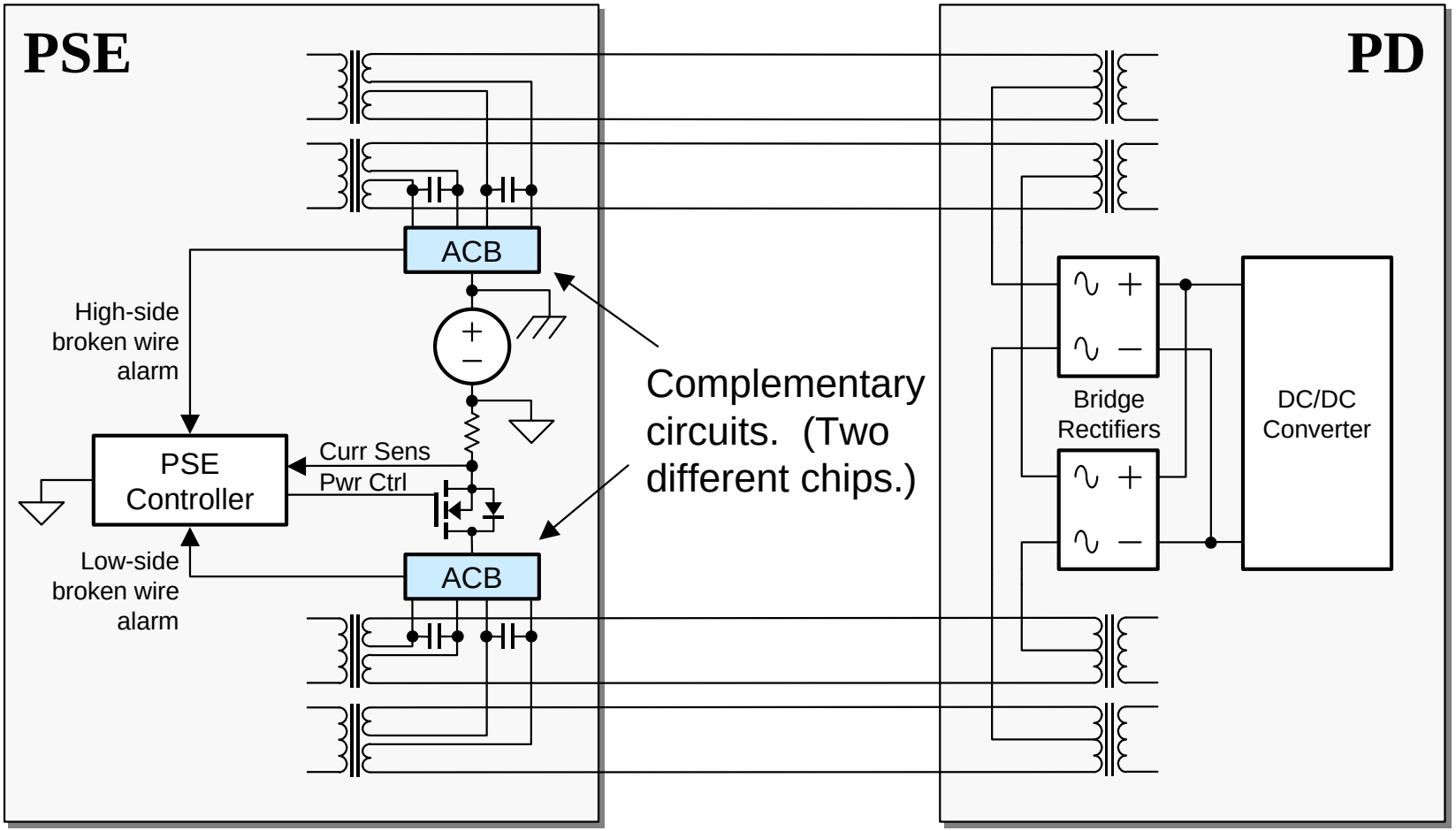
Goal: Increase I_{CUT} to the max safe capacity of CAT-5 cable.

Limiting Factors	Proposed Solutions
Current imbalances within a twisted-pair degrade transformer performance.	Add circuitry to actively balance the currents within pairs to better than ±8mA.
Cost/Complexity of 4-Pair power distribution.	Active current balancing between pairs. PD can use diode-ORing, PSE only needs one MOSFET per port.
Wire heating. Worst-case analysis becomes much harder when broken wires or bent connector pins are considered.	Add circuitry to detect broken wires, and turn off power to the PD. Garentees all wires are conducting equal currents.

Technical Feasibility

- System Block Diagram
- ACB Circuit Requirements
- Alternative ACB Topologies
- Vertical Bipolar Process
- Detecting Broken Wires
- SPICE Simulations

System Block Diagram

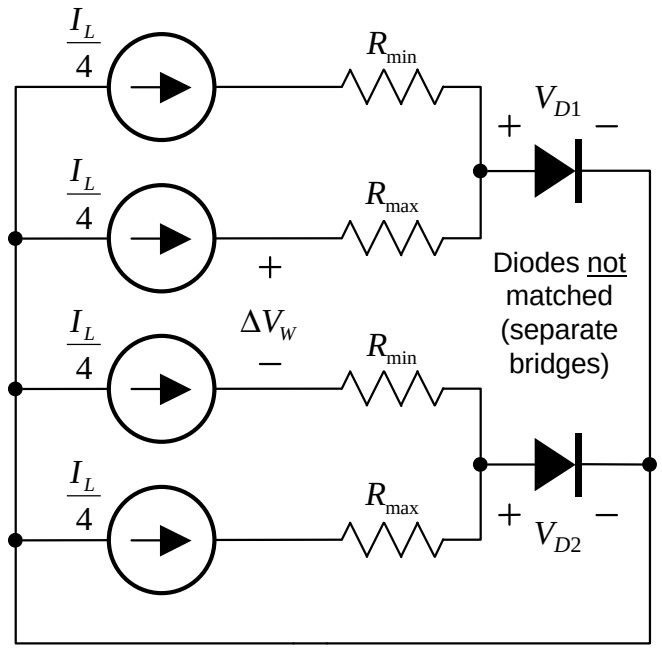


ACB Circuit Requirements

- 4-wire balance with up to 400mA per wire.
- Balance better than ±8mA, with up to 250mV difference between any two wires. (See next page for analysis.)
- Directly signals PSE controller chip to turn off power when one or more wires are broken.
- Low Cost
  - No external power supplies required
  - Minimal external components
  - Low complexity (minimum process steps)
  - Low power dissipation (small package, no heat sinks)

Worst-Case Differential Voltage

Assume ACB circuit forces equal currents on all 4 wires.



Worst-case differential resistance

$$R_{max} - R_{min} = 2\Delta R_T + \Delta R_W + \Delta R_C$$
$$= 2(0.03) + (9.60)(0.03) + 0.1 = 0.448\Omega$$

100m of 24AWG @ 50C (Table 33E.1)

Worst-case differential diode drop

Let I_{S1}=3.14e-7 I_{S2}=6.28e-7 T_1=300K T_2=280K I_L=1.6A

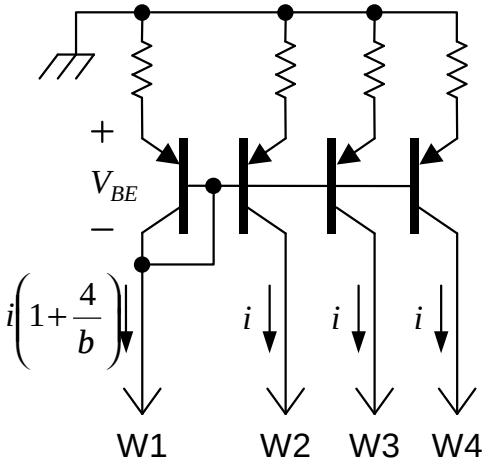
$$\Delta V_D = V_{D1} - V_{D2} = \frac{kT_1}{q}\left\{\ln\left(\frac{I_L}{2I_{S1}}\right) - \frac{T_2}{T_1}\ln\left(\frac{I_L}{2I_{S2}}\right)\right\} = 0.0442$$

Worst-case differential voltage seen at current mirror inputs

$$\Delta V_W = \frac{I_L}{4}\left(R_{max} - R_{min}\right) + \Delta V_D = \mathbf{223mV}$$

ACB Circuit Topologies

Basic Current Mirror

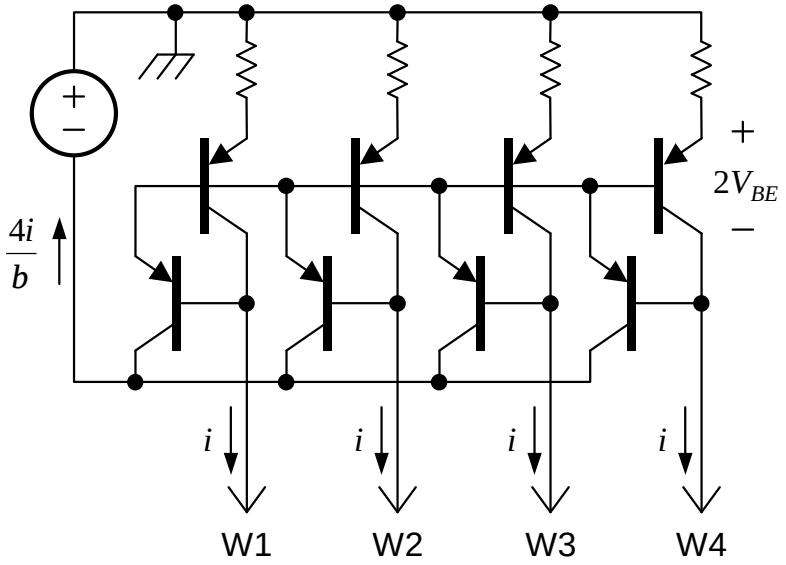


Problems:

•If W2,W3, or W4 breaks, current will still flow on W1. This can be detected and power shut off. But if W1 breaks, it looks like the PD has been connected. Can't tell the difference.

•Currents slightly unequal because *b* is finite.

"Symmetrical" Current Mirror



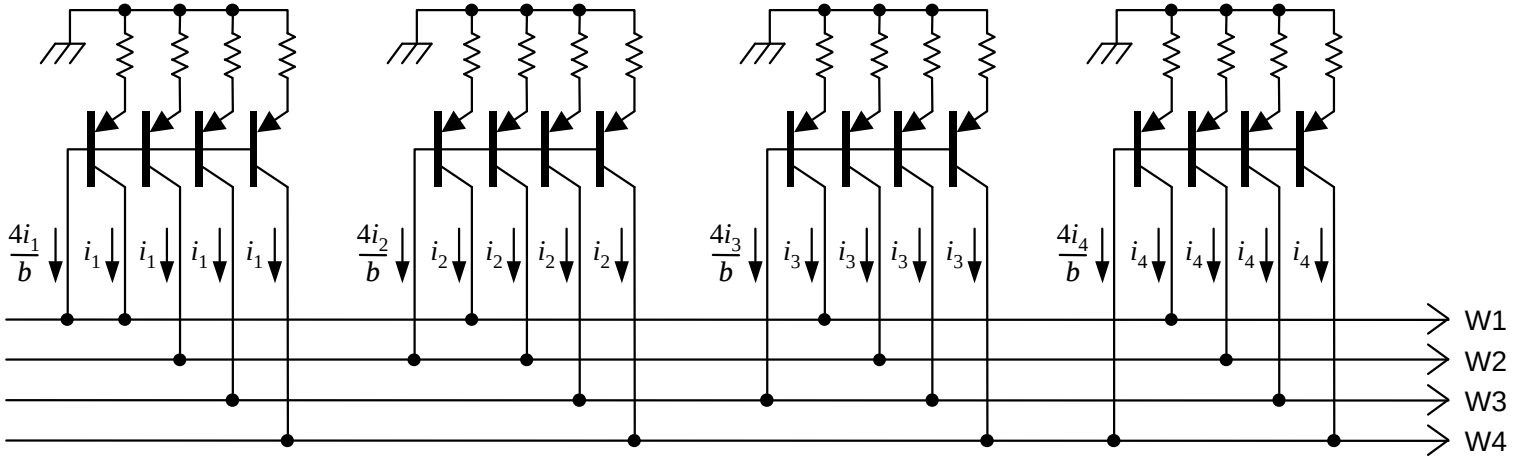
Problems:

•Twice the voltage drop means twice the power dissipation.

•External power supply required.

ACB Topologies (continued)

True Symmetrical Current Mirror (Circuit "A")



Even if the 4 mirrors don't share the load equally, the currents on all 4 wires remains nearly equal:

$$I(W1) = i_1 + i_2 + i_3 + i_4 + (4i_1/b)$$

$$I(W2) = i_1 + i_2 + i_3 + i_4 + (4i_2/b)$$

$$I(W3) = i_1 + i_2 + i_3 + i_4 + (4i_3/b)$$

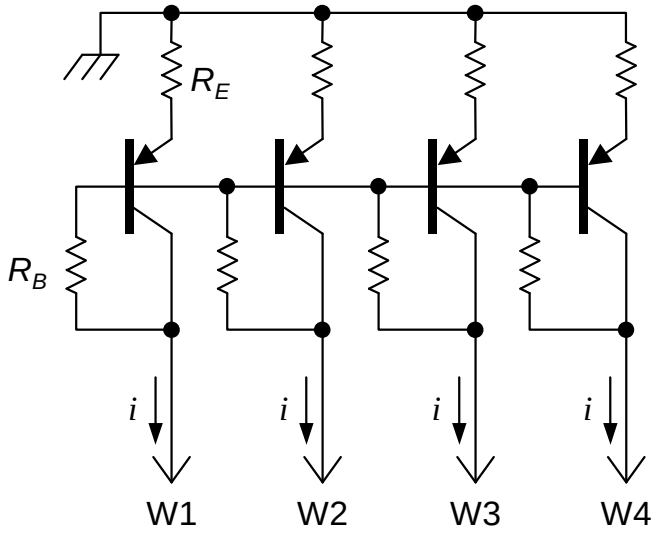
$$I(W4) = i_1 + i_2 + i_3 + i_4 + (4i_4/b)$$

Problems:

•Increased die area. Voltage differences on the wires makes $i_j \neq i_k$. The 4 mirrors don't share the load equally, so all transistors must be larger.

ACB Topologies (continued)

Alternative Symmetrical Current Mirror (Circuit "B") (Joseph DeNicholas)



Advantages:

- All transistors share equally.
- Die size might be smaller.

Problems:

- Higher power dissipation than Circuit "A"
- Requires large b.

Beta	P_D @ 1.6A
100	3.30
200	2.50
300	2.25

R_E=0.57Ω, R_B=100 Ω

(Circuit A: 1.39W @ 1.6A, R_E=1.5Ω, independant of Beta.)

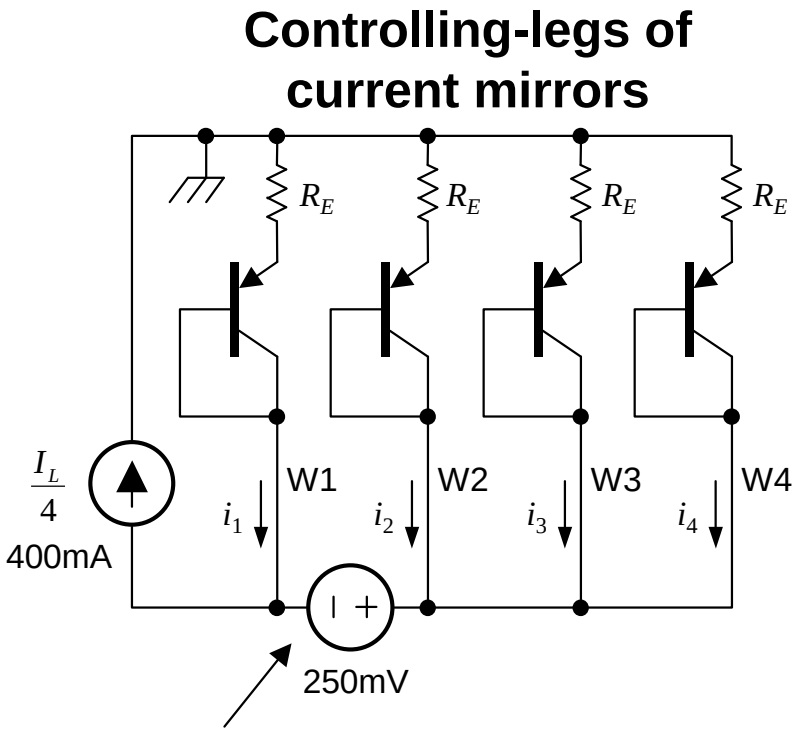
ACB Topologies (continued)

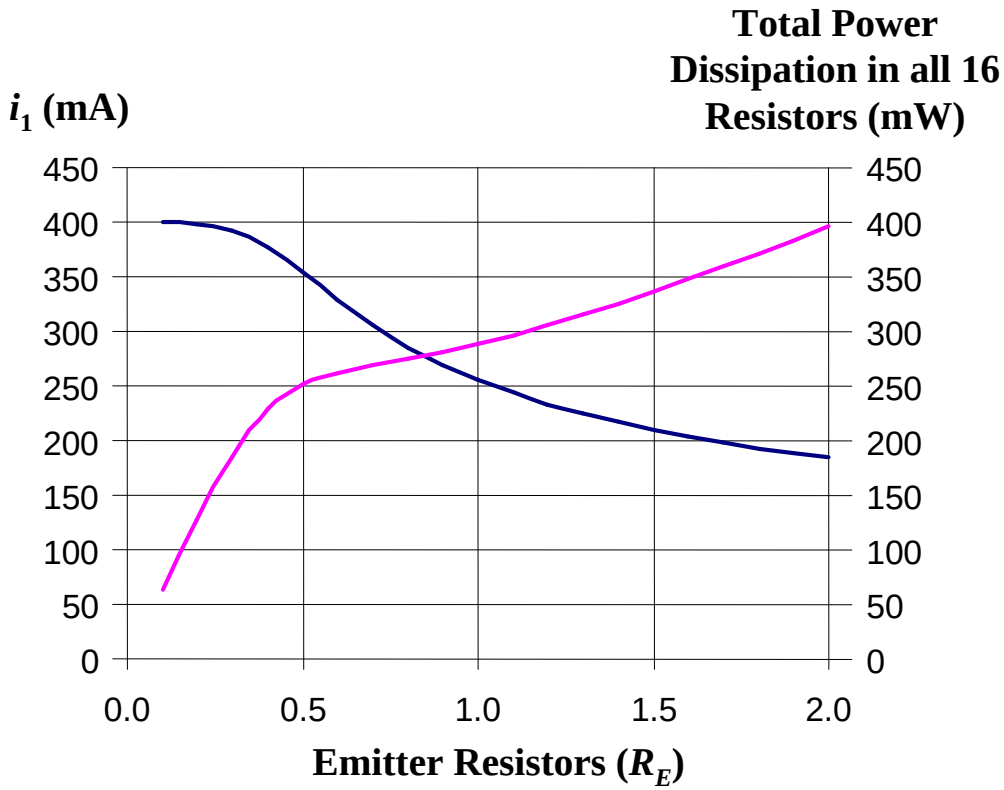
Bipolar vs. CMOS

Similar circuits could be implemented in CMOS, but the voltage drop, and power dissipation would be much greater.

To acheive similar voltage drops with CMOS, the power MOSFETs would need to be in the linear region (not pinch off). Accurate current-balancing can't be acheived by device-matching alone: active control circuitry (opamps) would be necessary. This entails the need for external power supplies.

Current Sharing In Circuit "A"



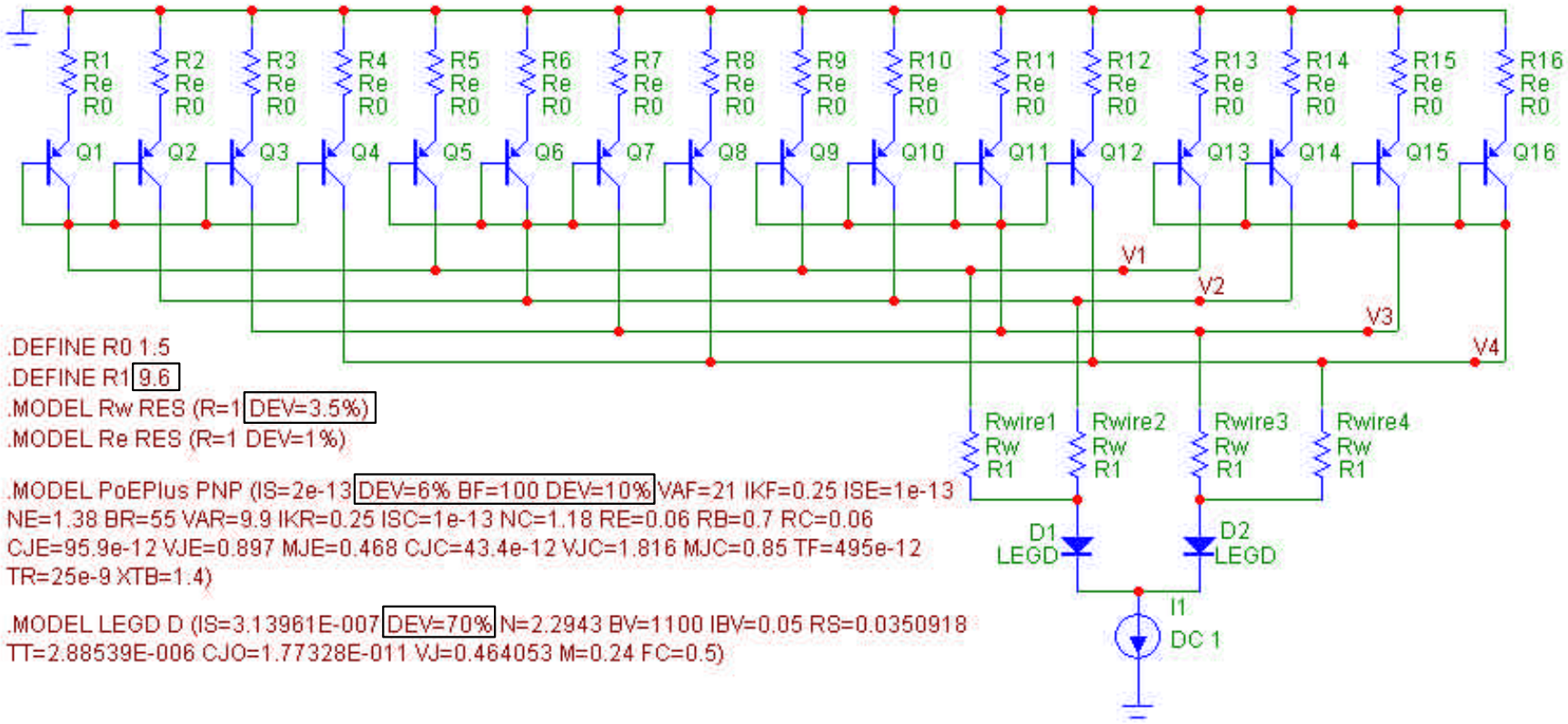


- Let $R_E = 1.5\Omega$
- Transistors must handle 200mA each before significant loss of gain (high injection effects).

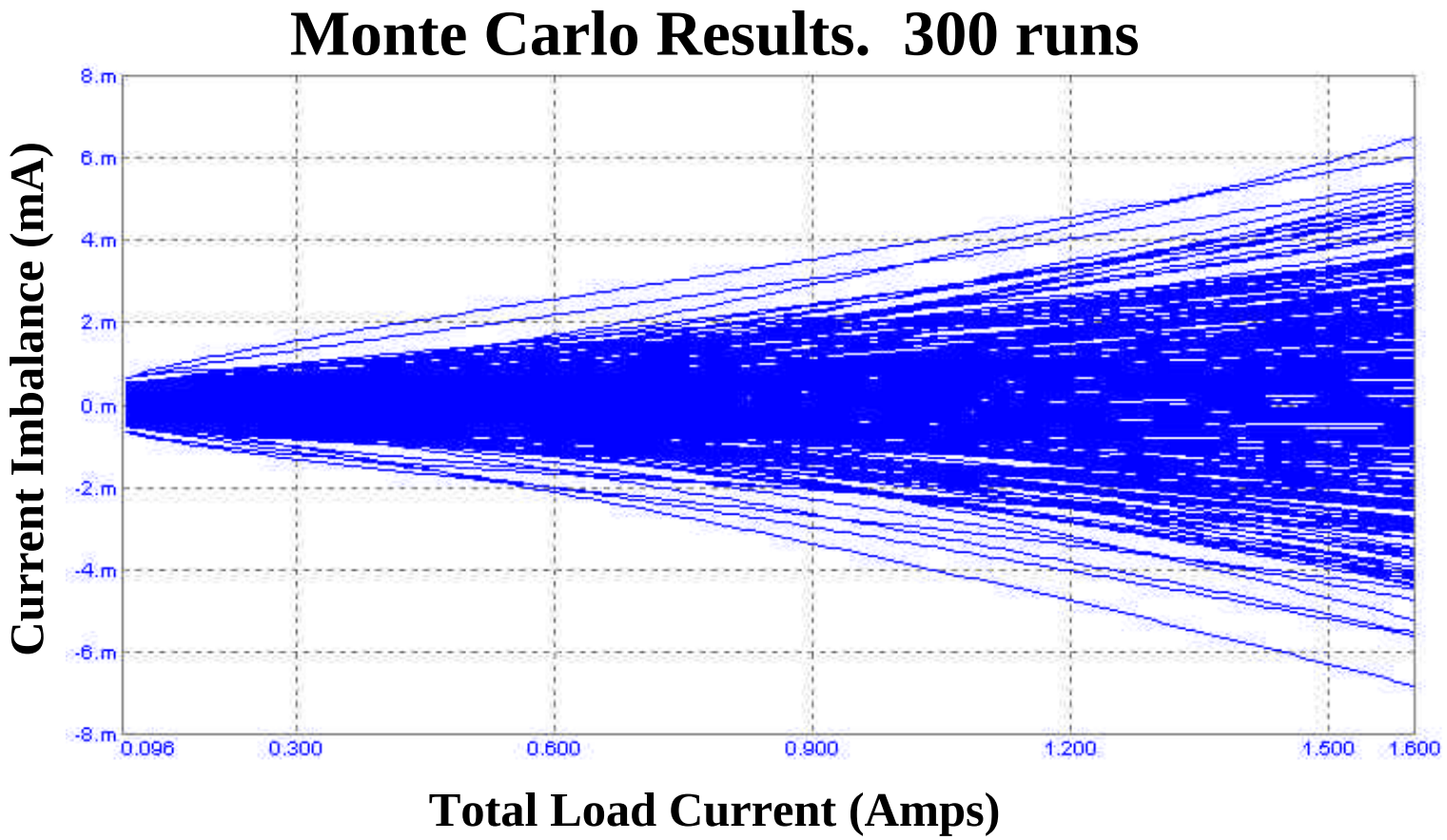
SPICE Analysis

- Selected Circuit A because of it's lower power dissipation.
- Chose PNP model for a Low-Sat off-the-shelf transistor and modified it:
  - Lowered Beta to 100 (was >300), and added 10% tol.
  - Added 6% tolerance to saturation current (equivalent to 2mV V_{BE} missmatch)
  - Did not attempt to add parasitic transistors.
- Chose off-the-shelf diode model. (From bridge rectifier used in some PoE applications. Added 80% tol on saturation current.
- Wire resistance is max for 100m of 24AWG at 50C. Added 3.5% tolerance.

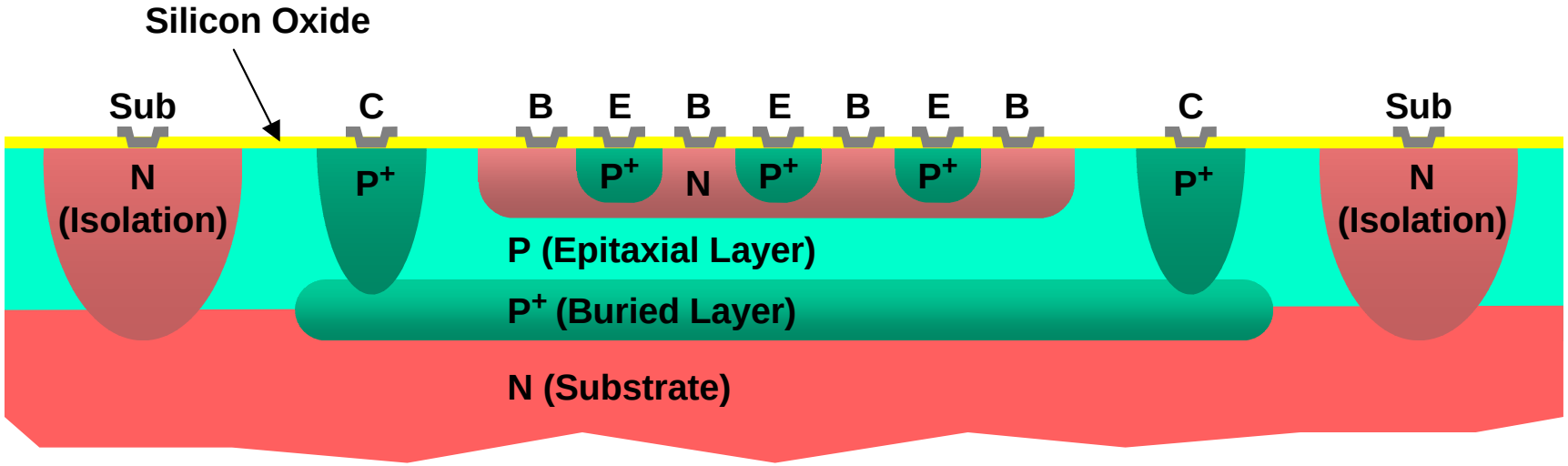
SPICE Model


R1 Re R0
R2 Re R0
R3 Re R0
R4 Re R0
R5 Re R0
R6 Re R0
R7 Re R0
R8 Re R0
R9 Re R0
R10 Re R0
R11 Re R0
R12 Re R0
R13 Re R0
R14 Re R0
R15 Re R0
R16 Re R0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
V1
V2
V3
V4
.DEFINE R0 1.5
.DEFINE R1 9.6
.MODEL Rw RES (R=1 DEV=3.5%)
.MODEL Re RES (R=1 DEV=1%)
.MODEL PoEPlus PNP (IS=2e-13 DEV=6% BF=100 DEV=10% VAF=21 IKF=0.25 ISE=1e-13
NE=1.38 BR=55 VAR=9.9 IKR=0.25 ISC=1e-13 NC=1.18 RE=0.06 RB=0.7 RC=0.06
CJE=95.9e-12 VJE=0.897 MJE=0.468 CJC=43.4e-12 VJC=1.816 MJC=0.85 TF=495e-12
TR=25e-9 XTB=1.4)
.MODEL LEGD D (IS=3.13961E-007 DEV=70% N=2.2943 BV=1100 IBV=0.05 RS=0.0350918
TT=2.88539E-006 CJO=1.77328E-011 VJ=0.464053 M=0.24 FC=0.5)
Rwire1 Rw R1
Rwire2 Rw R1
Rwire3 Rw R1
Rwire4 Rw R1
D1 LEGD
D2 LEGD
I1
DC 1

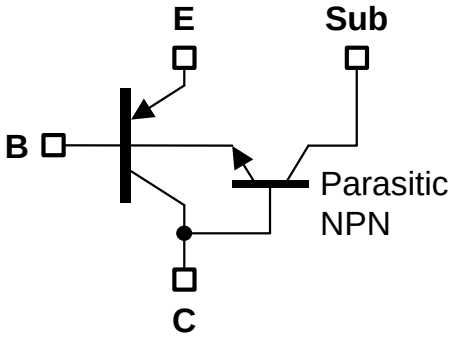
SPICE Results



Vertical Bipolar Process



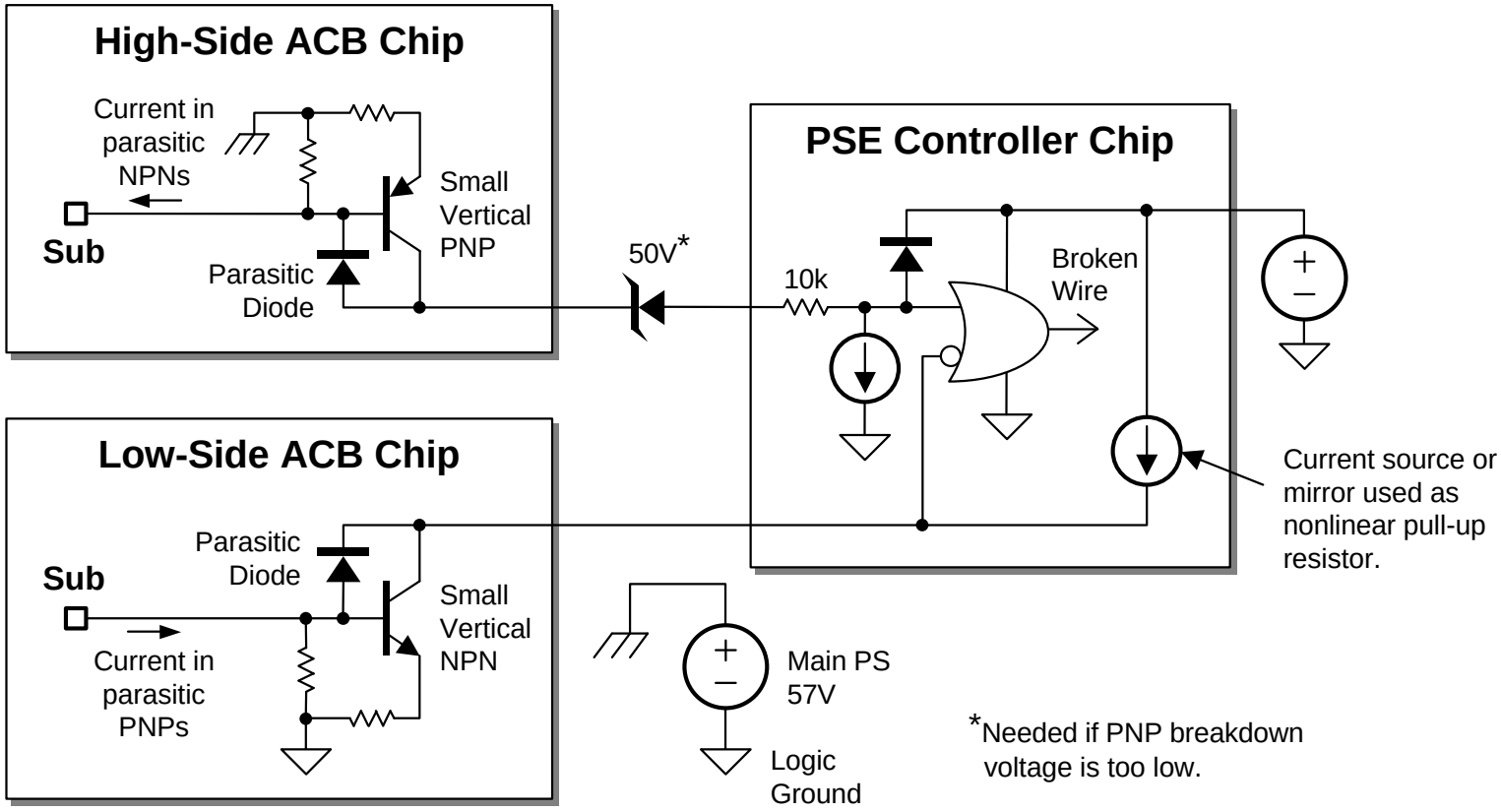
Equivalent Circuit



When the PNP is saturated, the parasitic NPN steals it's base current. Substrate current (normaly very small) increases dramatically.

Detecting Broken Wires

Broken wires ⇒ Saturated Transistors ⇒ Large Substrate Currents.
Simple circuits sense voltage drop on substrate-to-ground connections.



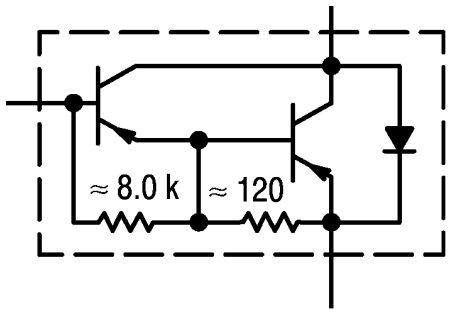
Estimation of Relative Cost

High-side ACB chip cost estimate based on comparison to off-the-shelf Darlington PNP:

Ratings:

$I_{C(MAX)}$=5A

Package: TO-220AB



- Similar die size
- Similar package – but fewer pins
- Similar process – but probably only one metal layer

Rough estimate: double the cost of this device.

Assume same for low-side ACB chip.

Estimation of Relative Cost

Other costs:

- Magnetics. Extra pins needed for split-windings. Package can't get larger (must fit behind RJ45), so pitch must shrink. Probably will have to use staggered pitch. Cost increase approx 15% (Hinrichs).
- PSE Controller chip. Need 2 extra pins per port for broken-wire detection inputs. Might be able to reduce it to 1 pin per port. Cost increase TBD.
- Discrete componets. Extra caps to couple the split-windings. Possibly Bob Smith terminations (probably pointless).
- Approx 60% more board space needed per port, because of ACB/BWD chips.

Bottom Line:

- Cost of PoE-related circuitry in PSE roughly doubles.
- Cost of PD not impacted.

Questions