An Extended Classification Protocol for PoE Plus

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Intro

Purpose of this presentation

To propose an extended classification protocol for PoE Plus that provides high resolution, is relatively simple, and is fully backward-compatible with 802.3af.

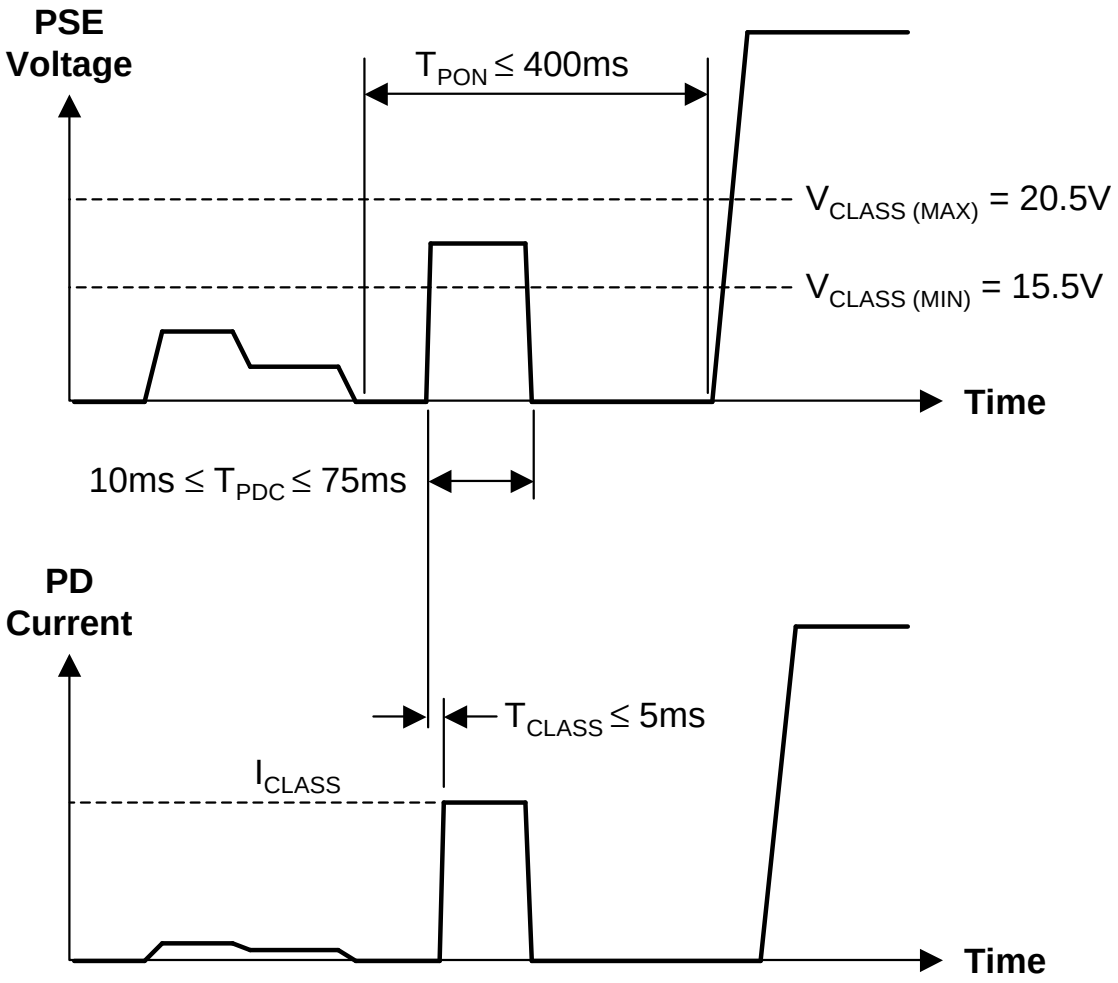
Terminology

- Equipment conforming to 802.3af are referred to herein as “af”. Example: “af-PD”.
- Equipment conforming to PoE Plus are referred to as “Plus”. Example: “Plus-PSE”.

Objectives

- Higher class resolution – many more power levels
- Mutual identification
  - Plus-PD can identify a PSE as either Plus or af
  - Plus-PSE can identify a PD as either Plus or af
- Backward-compatible with 802.3af
  - Detection signature resistance is not changed
  - af-PSE still able to classify Plus-PD
- Simplicity
  - Does not require serial communication between PSE and PD
  - Does not require smart PD
  - Does not require 4-pair wiring, but will work with either 2P or 4P

802.3af Classification Protocol

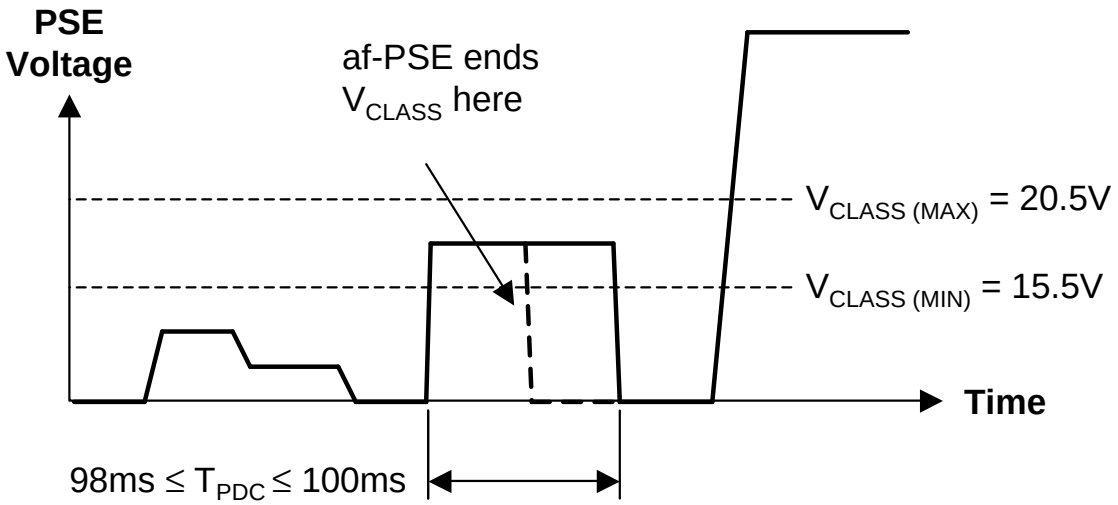


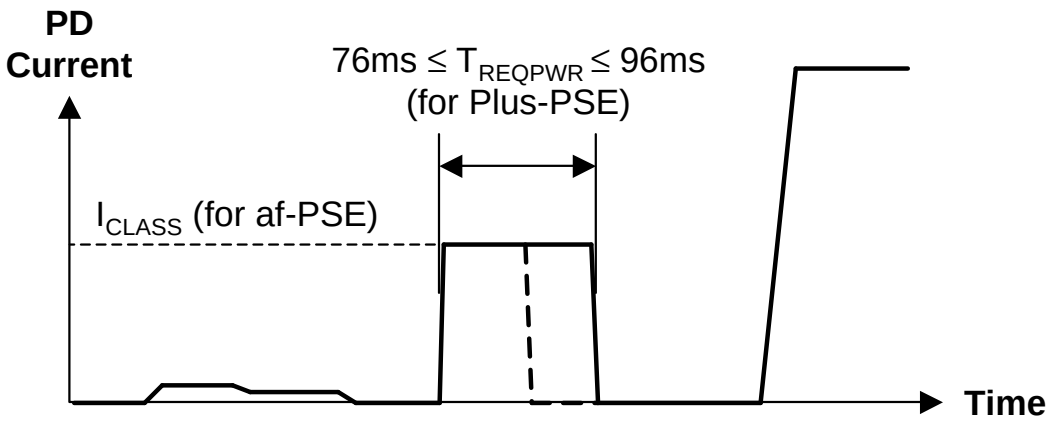
Waveform graphs are not to scale.

Protocol

1. PSE sources voltage between 15.5V and 20.5V.
2. PD recognizes voltage in this range as a class query. Responds within T_{CLASS} by sinking current I_{CLASS}.
3. PSE measures I_{CLASS}. Determines PD class from Table 33-4.

Extended Classification Protocol

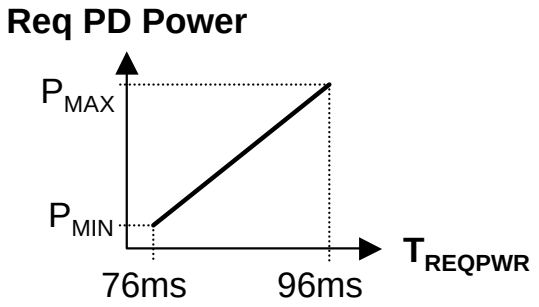




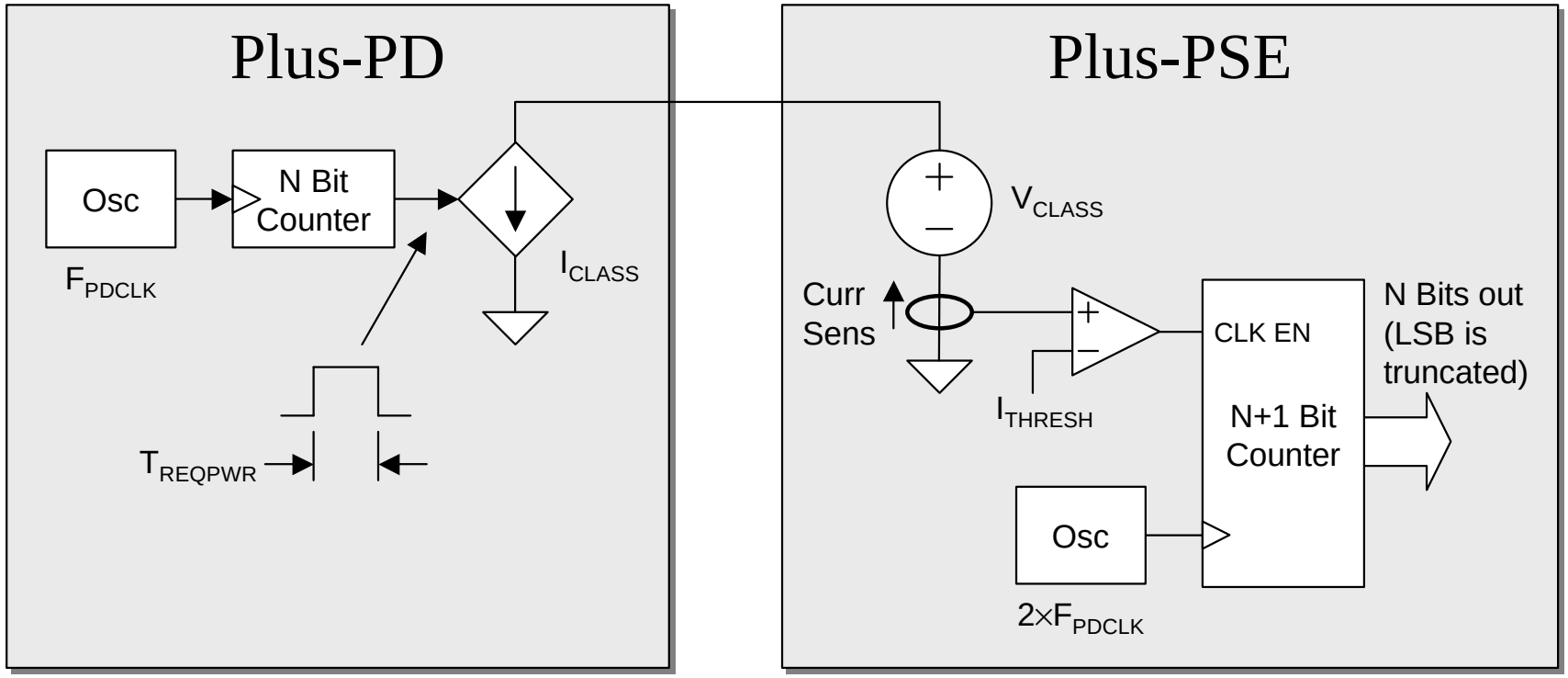
Waveform graphs are not to scale.

Protocol

1. Voltage and current levels are unchanged from 802.3af for backward-compatibility
2. Plus-PSE sources V_{CLASS} for longer period than af.
3. Plus-PD sinks I_{CLASS} for time period indicating its power requirements.
4. Plus-PSE measures T_{REQPWR} and determines PD requested power from linear equation.



Simplified Block Diagram



PSE clock freq is double PD clock freq to satisfy Nyquist

Higher Class Resolution

- It's easier to measure time precisely than voltage or current levels. A time-dependent scheme can attain high resolution at a lower cost.
- Example: Assume T_{REQPWR} range is 76 to 96ms, and timing resolution is 100µs. This yields 200 classes. If P_{MAX}=60W and P_{MIN}=0W, then the classes are only 300mW apart.
- Higher resolution is easily possible, limited by the frequency accuracy of the oscillators.

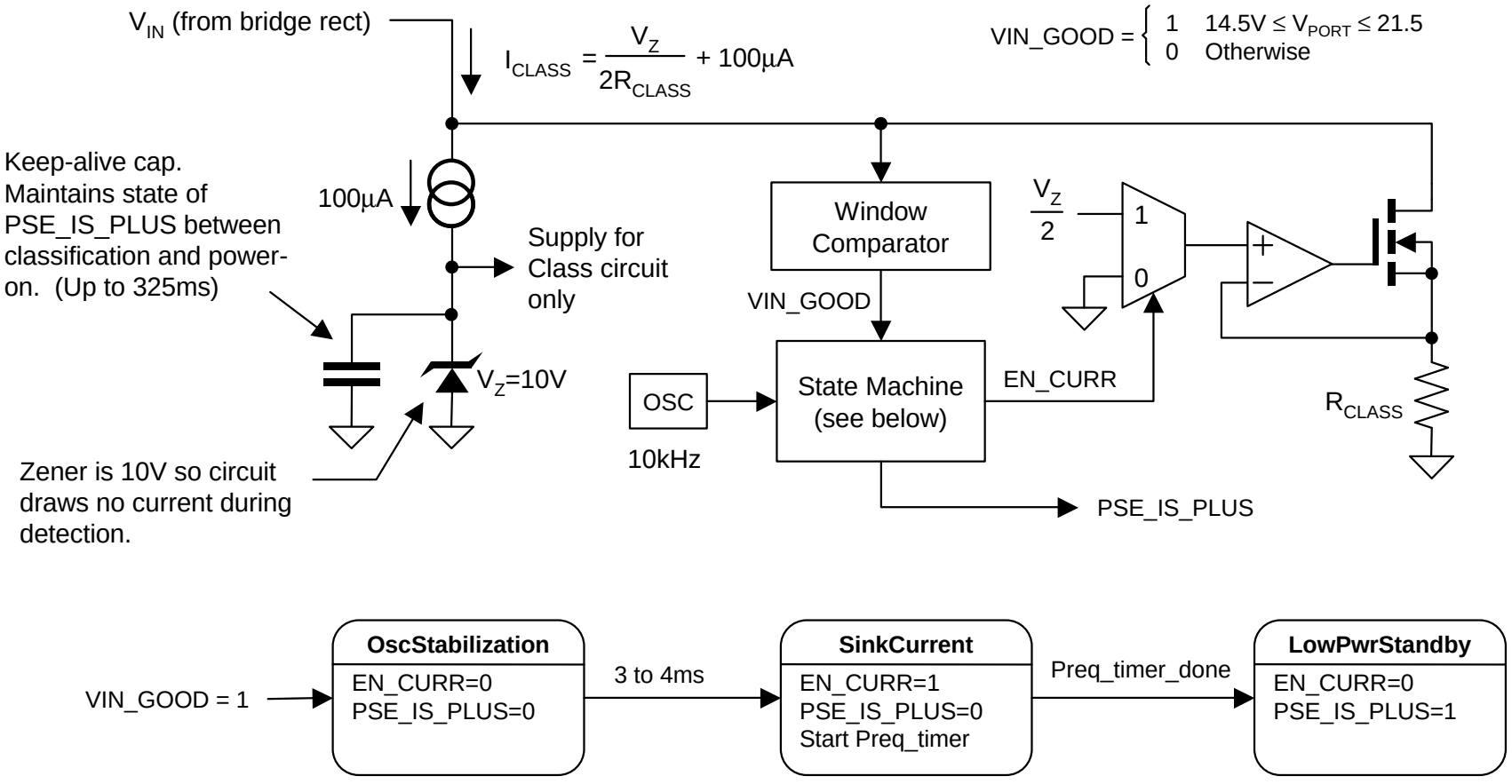
Mutual Identification

- How a Plus-PSE determines the PD type:
  - If the PD maintains I_{CLASS} as long as the PSE maintains V_{CLASS} then it's an af-PD.
  - If the PD cuts off I_{CLASS} before the PSE removes V_{CLASS} then its' a Plus-PD.
- How a Plus-PD determines the PSE type:
  - If V_{CLASS} lasts less than 76ms, it's an af-PSE.
  - If V_{CLASS} lasts longer than 76ms, it's a Plus-PSE.

Backward-Compatibility

- How a Plus-PSE looks to an af-PD:
  - The classification period lasts longer, but the PD operation is unaffected.
  - Everything else is the same.
- How a Plus-PD looks to an af-PSE:
  - There is no difference. Voltage and current waveforms look the same.
- Example: A Plus-PD that requires 8W
  - Set I_{CLASS}=28mA and T_{REQPWR}=78.7ms.
  - An af-PSE sees a Class 3 PD and allocates 15.4W (7.4W wasted).
  - A Plus-PSE sees a Plus-PD and allocates (78.7ms – 76ms)(60W/20ms) = 8.1W (only 0.1W wasted).

A Possible Plus-PD Design



Complexity and Cost

Any classification protocol that distinguishes 2^N classes will need N bits. This adds complexity and cost:

- How do you set the N-bits in the PD controller chip?

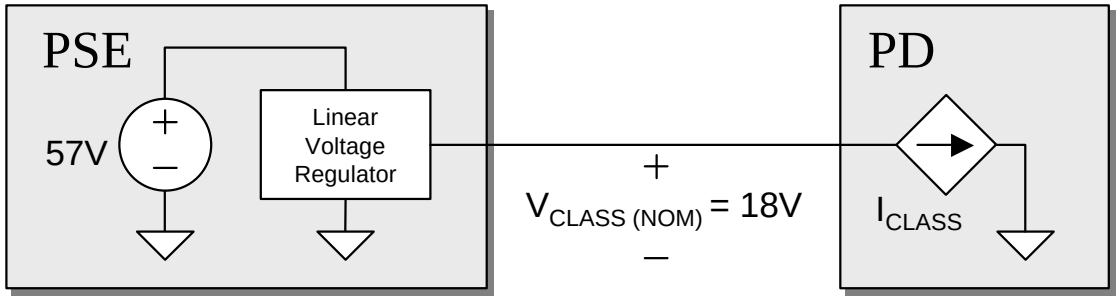
Possible Solution	Complexity Impact
N pins on IC	IC needs bigger package
Internal Nonvolatile memory	IC needs EEPROM and serial interface
External resistor	IC needs current source and A-to-D converter

- Impact of proposed method on PSE controller chip complexity:
  - Pin-count should be unaffected since it already has a CPU interface
  - State machine is more complex: Add N+1 bit counter
  - Class register needs more bits

Timing Accuracy

- The limiting factor is oscillator frequency accuracy
  - The PSE oscillator accuracy can easily be better than 0.02% (200ppm). Startup and stabilization times are not issues. A single low-cost crystal oscillator could serve all ports.
  - The PD oscillator needs to be cheap, easy to integrate on an IC, start up and stabilize quickly. Its accuracy will likely dominate the overall system timing accuracy. If its accuracy is 0.5% or better within 5ms, then we can get 200 classes.
- Other possible timing accuracy considerations
  - Class signature current slew rate. If the PD slews at least 10mA/µs then this will probably cause 2µs error at most.
  - Cable inductance. Won't be a problem if the current slew rates are kept reasonably low.

Thermal Considerations



Class	$I_{CLASS\ (MAX)}$ (From Table 33-11)	Max P_D in PSE Controller $P_D = (57V - 18V)(I_{CLASS})$	Max P_D in PD Controller $P_D = (18V)(I_{CLASS})$
0	4mA	156mW	72mW
1	12mA	468mW	216mW
2	20mA	**780mW**	360mW
3	30mA	**1170mW**	**540mW**
4	44mA	**1716mW**	**792mW**

- The proposed protocol extends the max time for V_{CLASS} from 75ms to 100ms. $P_{D\ (MAX)}$ would be the same, but longer time means higher junction temp.
- Recommend we don't implement Class 4.

Summary

- The proposed protocol achieves several goals:
  - Greatly increased class resolution
  - Mutual identification of Plus-PSE and Plus-PD
  - Backward compatible with 802.3af
  - Doesn’t require smart PD or 4P wiring
- Implementation seems very feasible
- Issues that need further study:
  - How many classes are really needed?
  - Cost and complexity impact on PSE and PD designs
  - Thermal considerations

Questions