Alternate PD Detection Proposal

IEEE 802.3 PoE Plus Study Group

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Alternate PD Detection Method

Goals

- No changes to the PD design
- Removal of DC components in the detection process
- Enable AC coupling
- Removal of level shifting dc errors
- Removal of DC offsets

Overview

Current detection method incorporates measuring the signature of a PD with a DC voltage. By measuring the same load with a transitory voltage and recover the AC from it. The errors associated with level shifting, base line wander and other dc offsets can be eliminated.

Since the measurements are dynamic and not DC, the measuring device may be AC coupled.

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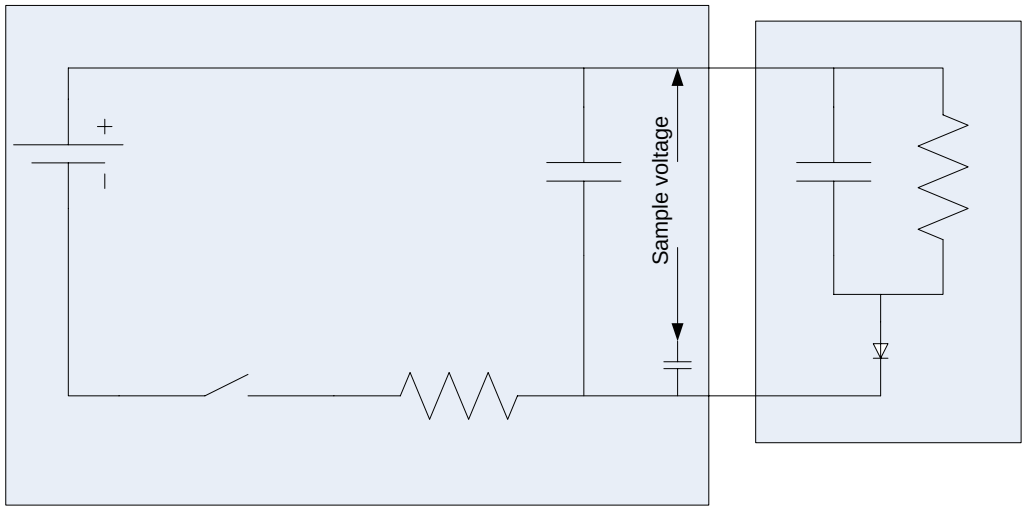
Consider the following circuit



Where

R1 is required by Section 33-2-5

C1 satisfies section Table 33-5 line 18

R2 is the detection value Table 33-2 line 7

C2 is optional per Table 33-2 line 10

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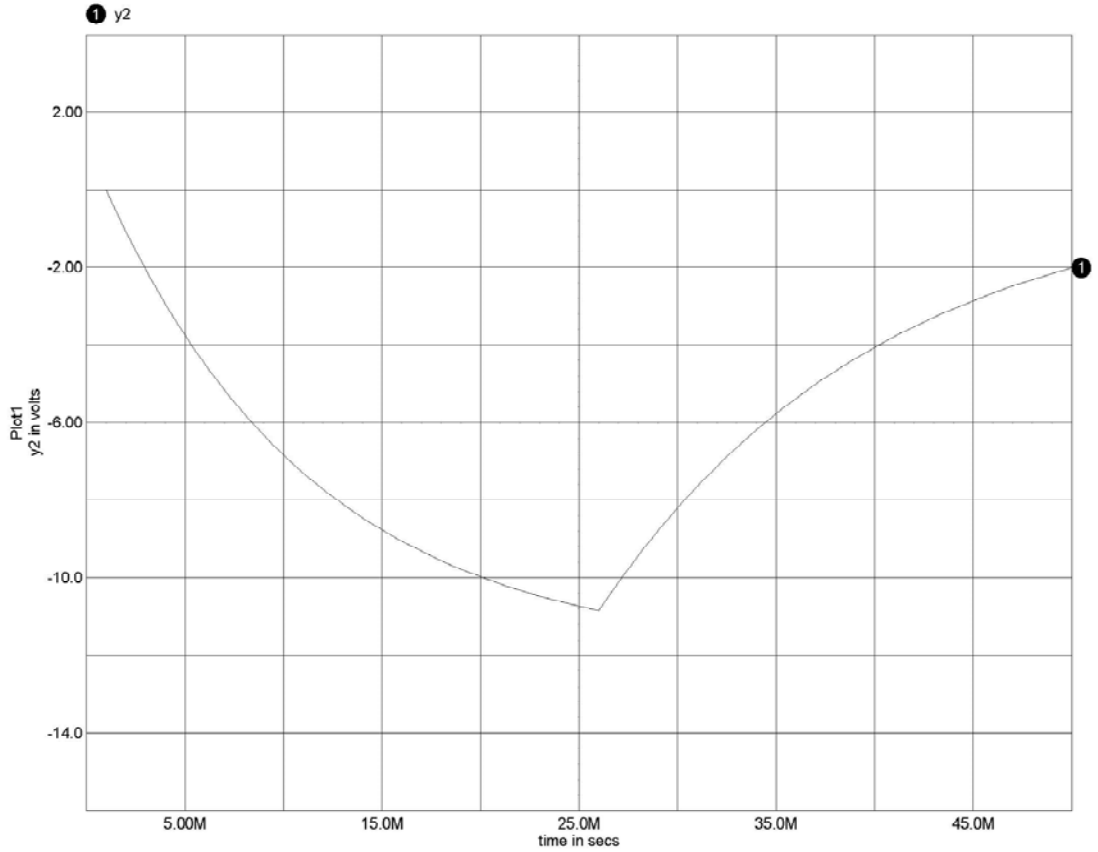
When the switch is closed and then opened the following wave form is generated



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Elimination of DC components

Math

The rise and fall time are classical exponential rise and fall times.

And $$\frac{d}{dx}(\exp(x) + \text{constant}) = \exp(x)$$

Therefore by taking the first derivative the dc affects can be eliminated or the affect be minimized and the original shape maintained. Commutation diodes' voltage drop are mainly DC and their effect is minimized.

In the sampled (digital) domain (first order difference)

$$\Delta V(n) = \left(V_{sample}(n) + DC\right) - \left(V_{sample}(n-1) + DC\right)$$

$$= \left(V_{sample}(n)\right) - \left(V_{sample}(n-1)\right)$$

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Digital circuit implementation

To determined the waveform in the digital domain minimizing the DC offset

- First the envelope is sampled N times. This may be done on the front, back or both edges.
- Secondly the samples are differentiated. In the digital domain this is accomplished by the first order difference.
- Finally the differentiated signal conforms to the correct exponential wave shape using the change (first order difference) in voltage calculations.

This process may be implemented with a small inexpensive microcontroller and an a/d converter similar to those available from TI, Microchip and in standard IC processes.

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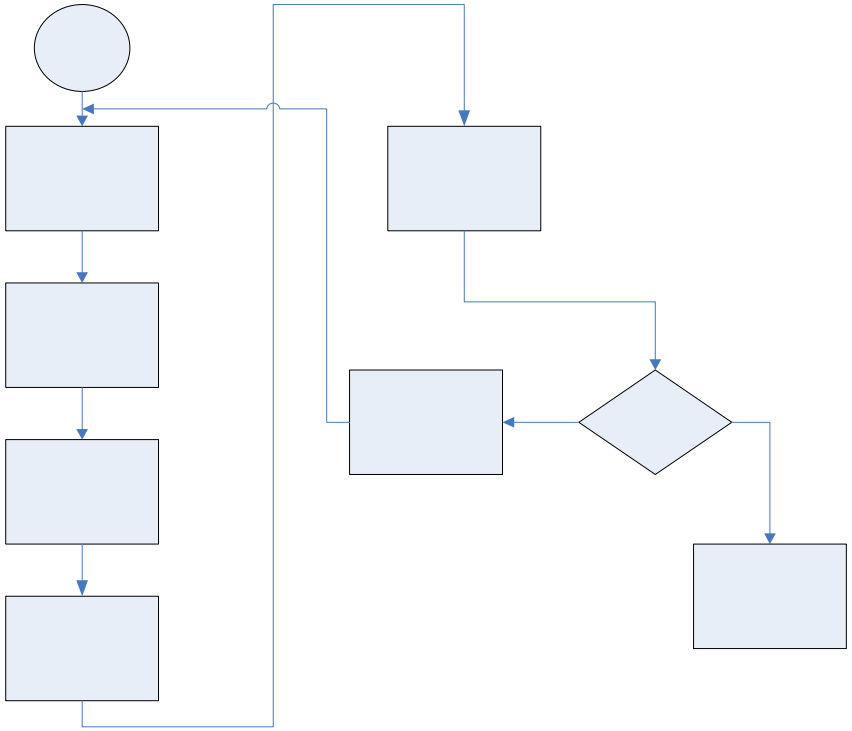
Flow Diagram



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Design considerations

1. C1 must be large enough to swamp out the variations of C2.
2. A clamp has to be provided to keep the voltage from exceeding 20V when the load is not present
3. When AC coupling, adequate time between events is needed to allow all capacitors to discharge.
4. Time must be allowed at switch turn on time to allow for the waveform to get beyond the discontinuity of the commutating diodes.

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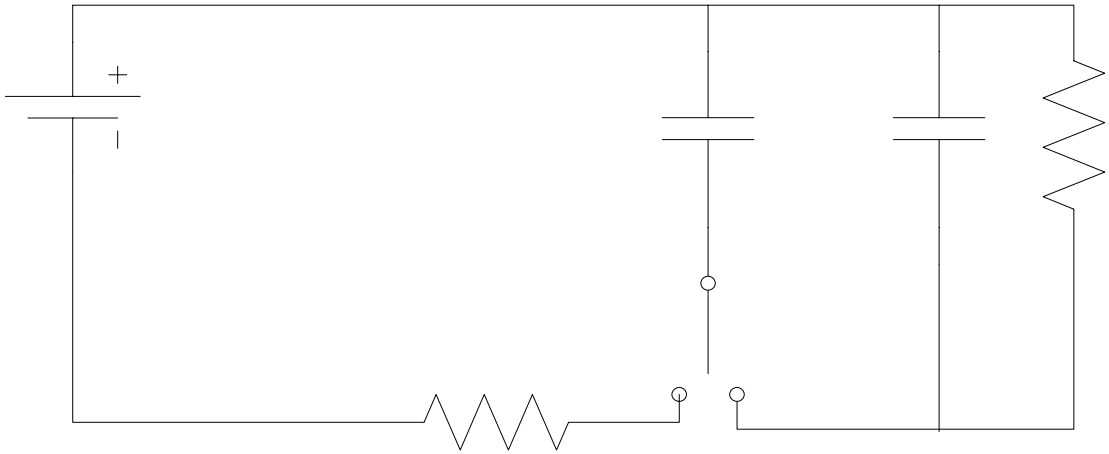
Corollaries

1. An alternate energizing method would be to charge a capacitor, then switch on the load and measure the discharge rate of the circuit.



2. R1 may be replaced with a current source making the first order differences a constant. This method is a simpler calculation, but may not be a robust as a more complicated wave shape.

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