GMII Electrical Specification

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Dave Fifield
1-408-721-7937
fifield@lan.nsc.com

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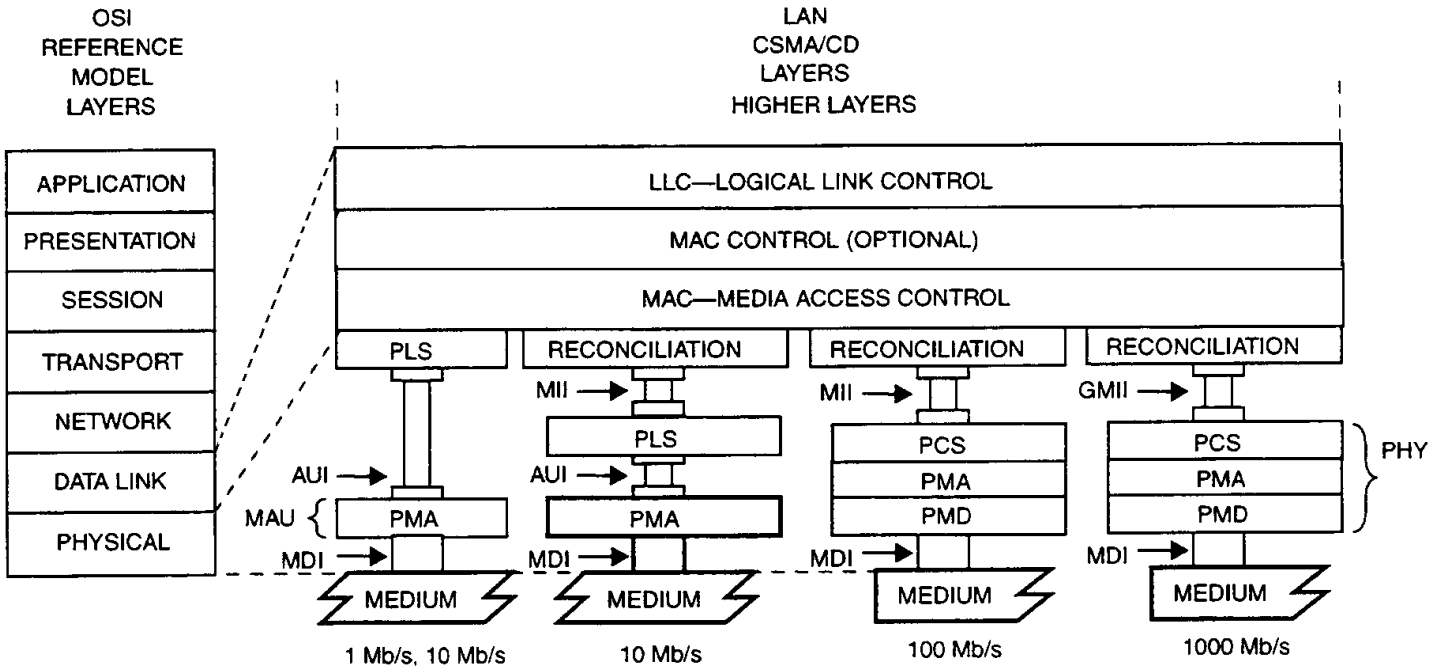
GMII Electrical Specification - Goals

- Compatibility with ANSI TR/X3.18-199x Revision 2.3 Fibre Channel - 10-bit Interface specification
- Compatibility with IEEE 802.3u Clause 22.4 MII Electrical Characteristics
- Manufacturable/Implementable using current technology

Why Compatibility With 10b and MII?



*** Allows us to use current technology for 1000Mb/s and provide backward compatibility with 10/100 Mb/s**

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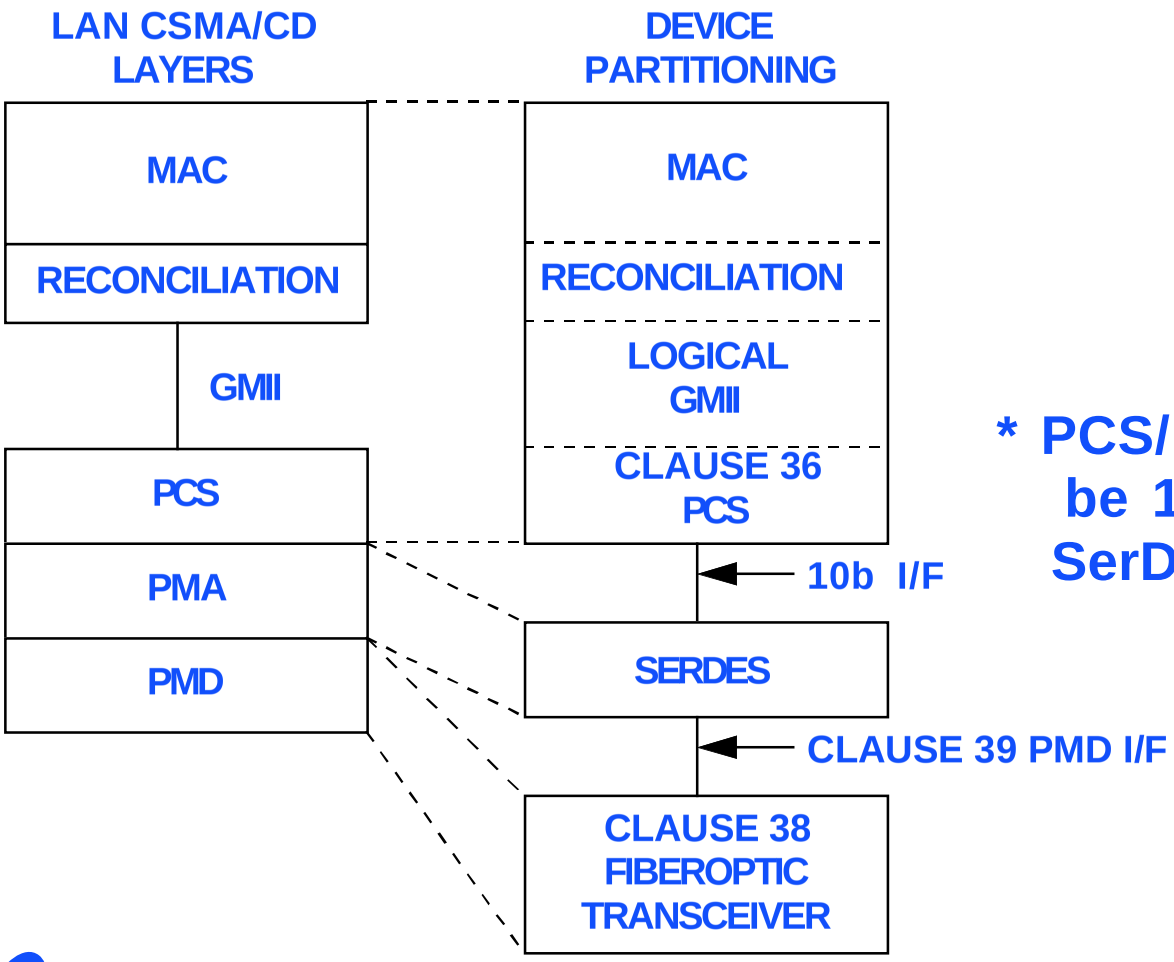
1000BASE-X Implementations



*** PCS/PMA interface must be 10b compatible so current SerDes devices can be used**

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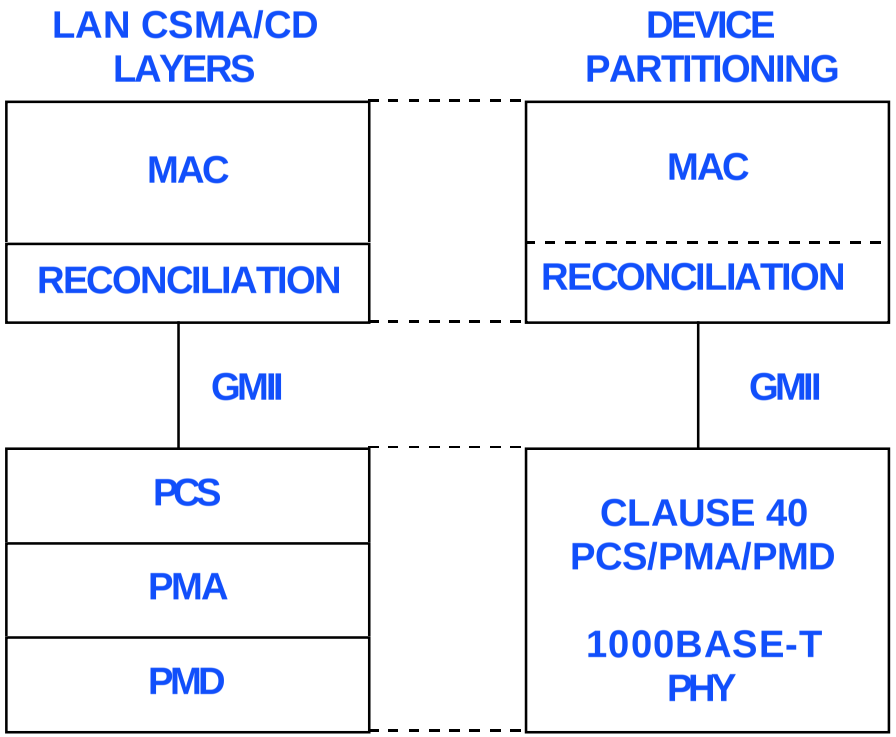
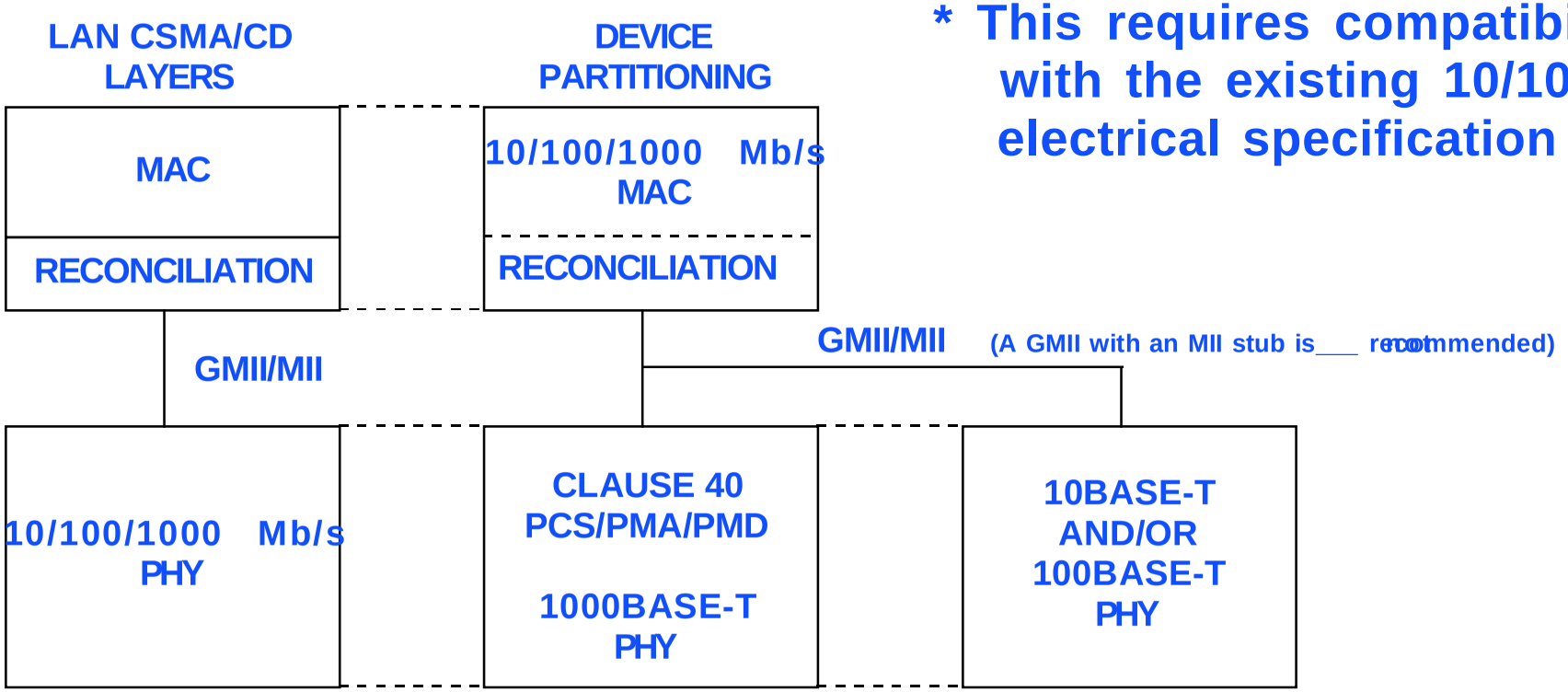
1000BASE-T Implementations



* GMII Electrical Specification is required to ensure vendor interoperability
* Sensible to make it compatible with 10b Electrical Specification so MAC device can be the same one used for 1000BASE-X (but with the 8b/10b PCS bypassed)

Mixed 10/100/1000BASE-T Implementaions

* Multi-speed MACs are likely to be implemented
* This requires compatibility with the existing 10/100 MII electrical specification



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10b Electrical Specifications

- TTL/CMOS input and output compatible
- Tolerance for mismatched input levels is optional
  - Eg. a 5V output driving a 3.3V input
  - Devices that meet this specification but are <u>not</u> tolerant of mismatched input levels are still regarded as compliant

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{OH}	Output High Voltage	I_{OH} = -400uA	V_{CC} = Min	2,4	3,0	V_{CC}	V
V_{OL}	Output Low Voltage	I_{OL} = 1mA	V_{CC} = Min	GND	0,25	0,6	V
V_{IH}	Input High Voltage			2,0	-	V_{CC}[1] + 10%	V
V_{IL}	Input Low Voltage			GND	-	0,8	V
I_{IH}	Input High Current	V_{CC} = Max	V_{IN} = 2,4V	-	-	40	µA
I_{IL}	Input Low Current	V_{CC} = Max	V_{IN} = 0,4V	-	-	600	µA
C_{IN}	Input Capacitance			-	-	4,0	pf
t_R	Clock Rise Time	0,8V to 2,0V		0,7	-	2,4	ns
t_F	Clock Fall Time	2,0V to,8V		0,7	-	2,4	ns
t_R	Data Rise Time	0,8V to 2,0V		0,7	-	-	ns
t_F	Data Fall Time	2,0V to 0,8V		0,7	-	-	ns

[1] Refers to the driving device power supply.

Source - ANSI TR/X3.18-199x Revision 2.3 Fibre Channel - 10-bit Interface Specification

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MII Electrical Specifications

- TTL/CMOS input and output compatible
- MII receivers required to be tolerant of all input potentials from 0V to +5.5V and (15ns) transients from -1.8V to +7.3V
  - More stringent than the 10b specification

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4				V
V_{OL}	Output Low Voltage	I_{OL} = 4mA			0.4		V
V_{IH}	Input High Voltage		2.0				V
V_{IL}	Input Low Voltage				0.8		V
I_{IH}	Input High Current	V_i = 5.25V			200		uA
I_{IL}	Input Low Current	V_i = 0.00V			-20		uA
C_{in}	Input Capacitance				8		pF
d_t	MII Cable Delay Variation (Skew)				0.1		nS

Source - IEEE 802.3u Clause 22.4, MII Electrical Characteristics

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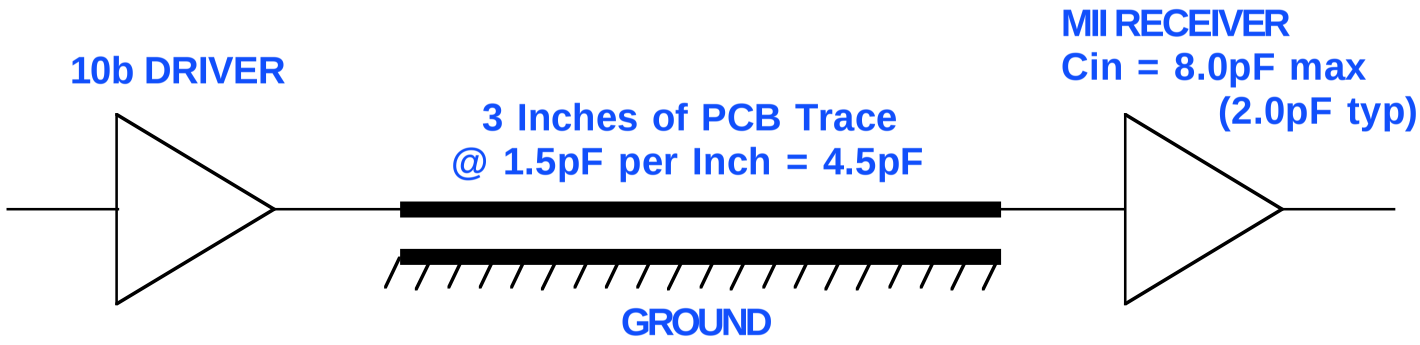
Combining the Electrical Specifications

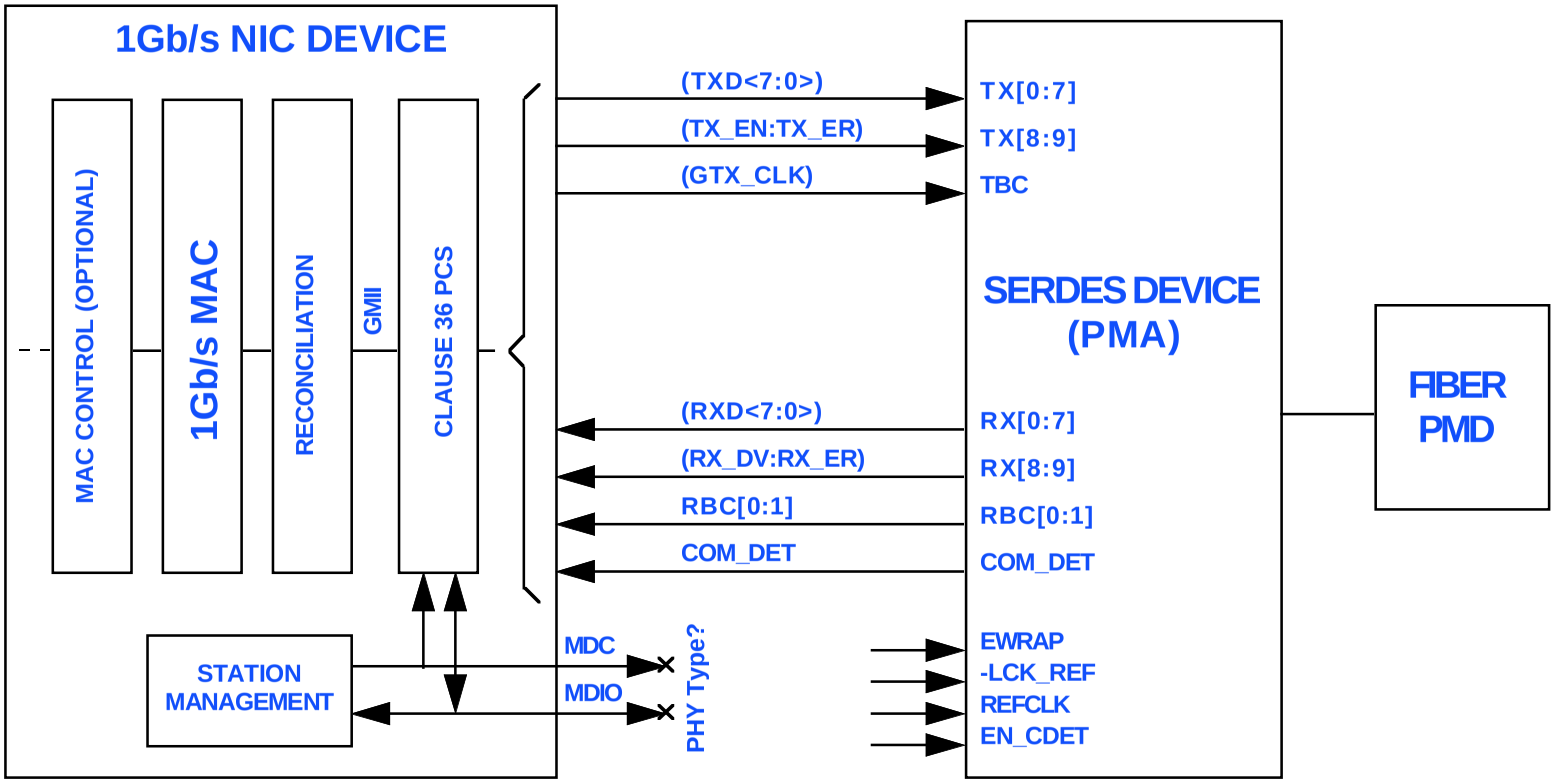
- Not practical to force the higher current MII drive specifications on existing SerDes devices
  - GMII specifies no connector or cable - 10b drive levels are sufficient
- With a voluntary restriction (recommendation?) to use GMII in MII mode only over short, matched, PCB traces, the 10b specification will provide adequate compatibility with existing 10/100 Mb/s PHY devices
  - This restriction cannot be standardized (define “short”!?)
  - Could add a note in Clause 42 System Considerations

10b/MII Compatibility

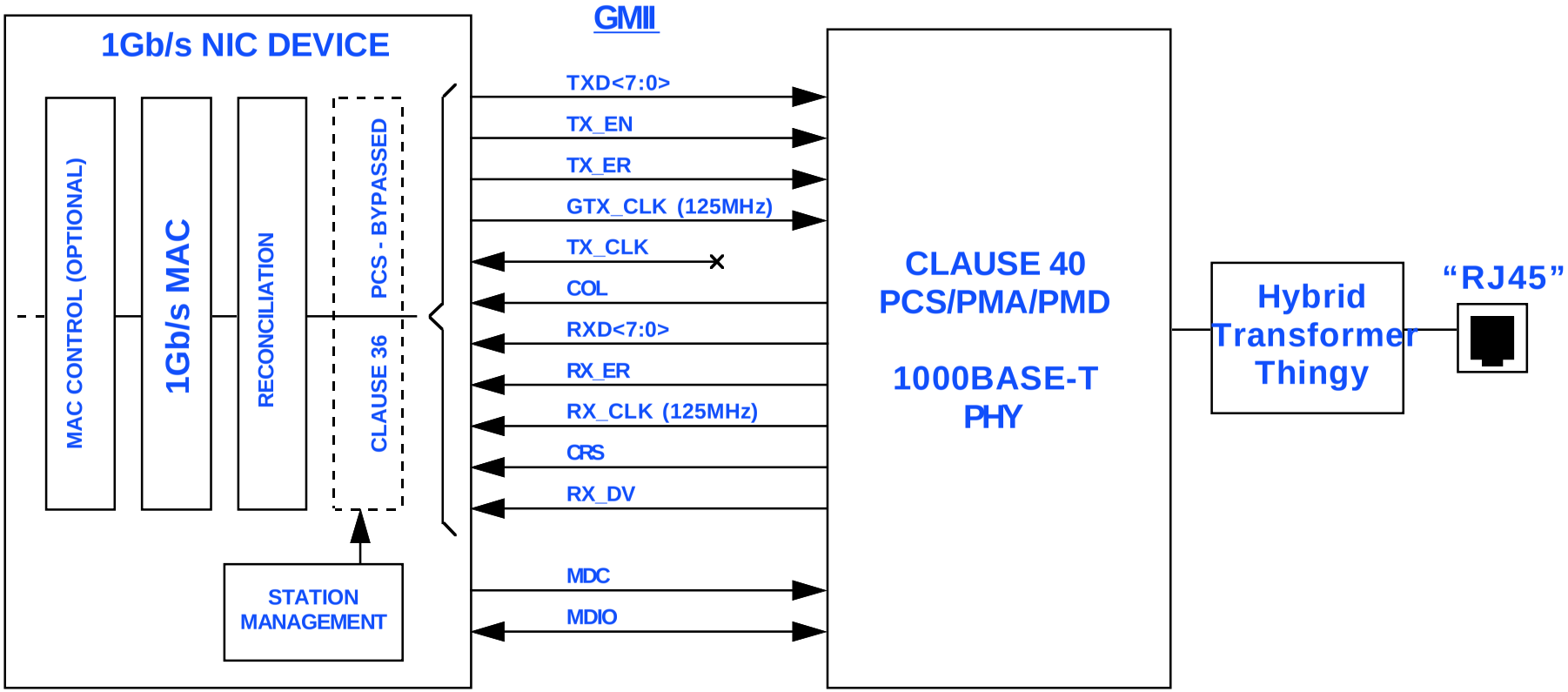


- Since the transmission line is very short, it can be treated as as a lumped capacitance output load
- Total load on the 10b driver = 12.5pF max, 6.5pF typ
- All 10b AC specifications are specified with an output load of 10pF
- Ran out of time to do the math, sorry!
- All the indications are that this should work

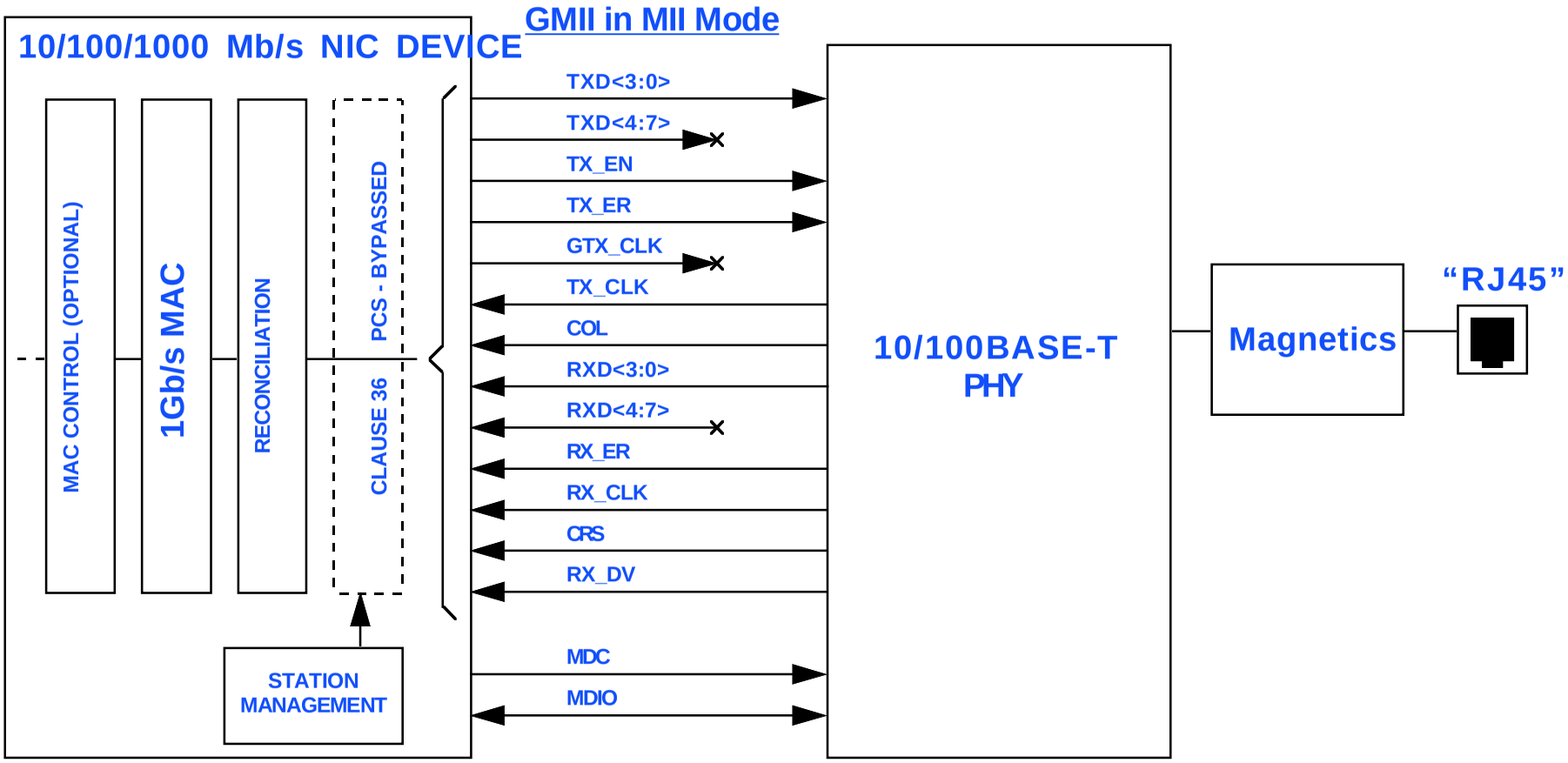
Hooking up a 1000BASE-X PHY



Hooking up the GMII - 1000BASE-T



Hooking up the GMII - 10/100BASE-T



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GMII - Work to do

- Complete math to prove 10b/MII compatibility
- Using Asif Iqbal's work on timing as a basis, write Clause 35.3 Signal Timing Characteristics
  - Include worst case permissible delay, skew and capacitance of the GMII transmission medium (PCB trace specifications)
- Using 10b specification as a basis (as it already is in Draft D1), edit Clause 35.4 Electrical Characteristics
  - Signal termination
  - DC specifications
- Speed selection and Fiber PHY type selection method
  - Selector pins on GMII?