

Gigabit Ethernet Serial Link Codes

Proposal for serial link codes and receiver / transmitter states
based on the PCS protocol requirements.

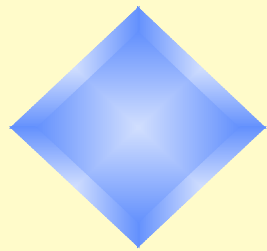
Contents

Link startup codes
Automatic link configuration data
SOP/EOP and Idle codes
Data and invalid character codes
Link synchronization states
and protocols

IEEE 802.3z Gigabit Task Force
July 9, 1996
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amdahl Corp.

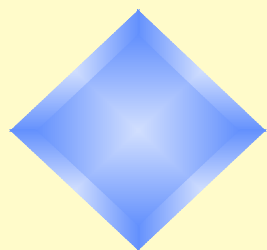
The following companies have indicated their support for the concepts outlined in this proposal (in alphabetical order):

3Com, Amdahl, Cisco, Compaq, Granite, Packet Engines, Sun, VLSI
Logic, and Xaqti.



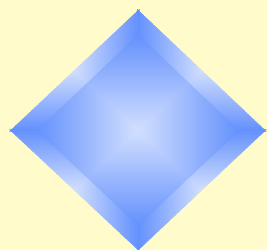
Changes in Revision 3

- ❖ **Howard Johnson** - Corrected legend for S, T, H and R codes to indicate that running disparity is unchanged
- ❖ **Howard Johnson** - Change H (error code) to **not** replace R (carrier extension) when an invalid transmission character is detected.
 - H shall be used to replace invalid data characters and Start (S) and End (T) delimiters
- ❖ **Steve Haddock** - Packet burst support. R **separates** packets within a burst.
 - The **positive** version of the S delimiter is now utilized
- ❖ **Steve Haddock** - Optimization of 8B10B codes assigned to define Ordered Sets.



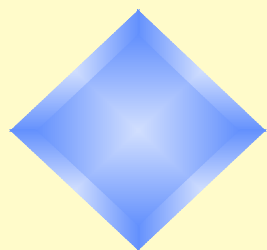
High-Level Assumptions

- ◆ Codings are based on 8B10B data codes (Dx.y) and special control characters (Kx.y) as defined in ANSI X3.230 FC-PH (Fibre Channel) Clause 11.
- ◆ Codings should take into careful consideration the error detection properties of code words selected.
- ◆ Codings are required for all primitives specified for the link startup sequence.
- ◆ Codings should provide sufficient coding space for all automatic capability detection parameters and shall be similar in nature to the base capability register defined in IEEE 802.3u clause 28.
- ◆ Automatic capability detection codings should allow for future expansion of the associated protocol.
- ◆ Codings are required for idle codes as well as a defer indication to be signaled during the idle sequence.
- ◆ Codings are required for IEEE 802.3 packets and bursts of packets during a carrier event.
- ◆ Codings are required for packet start and end delimiters.
- ◆ Coding is required for a bad packet information indication.
- ◆ Coding is required for an indication which allows the carrier to be extended.
- ◆ Coding is required for an indication which ensures that packet or carrier extension always concludes on an odd-numbered character.



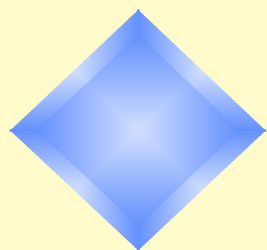
Nomenclature

- ◆ One or more data codes and special characters are grouped into transmission words.
- ◆ Special transmission words called ordered sets are defined.
- ◆ Packet delimiter ordered sets are used to mark packet boundaries.
- ◆ Signal ordered sets are used to signal events.
- ◆ Sequence ordered sets are repeated ordered sets used to signal states, carry information and operate in environments with relatively (to frames) high error rates.
- ◆ The link is not considered usable until Link Initialization is complete.
- ◆ Synchronization is achieved when the receiver identifies the same transmission word boundary on the received bit stream as that established by the transmitter at the other end of the link.
- ◆ The detection of Invalid Transmission Words is an indication that a receiver is out of synchronization.
- ◆ The clock recovery system in a receiver shall have sufficient hysteresis to prevent a single transmission error from causing it to go out of synchronization.
- ◆ A Loss_of_Synchronization Procedure defines the method by which the receiver changes from the Synchronization_Acquired state to the Loss_of_Synchronization state.
- ◆ The first transmission character of an ordered set transmitted over an operational link is transmitted in an even-numbered character position. Subsequent characters continuously alternate as odd and even-numbered characters.



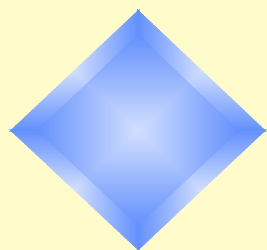
8B10B Transmission Code

- ❖ 8B10B transmission code provides the following functions:
 - Improves transmission characteristics
 - Enables bit-level clock recovery
 - Improves error detection
 - Separates data symbols from control symbols
 - Derives bit and word synchronization
- ❖ 8-bit data bytes are encoded as 10-bit **Data Characters**.
- ❖ 12 **Special Characters** are defined for special signaling.
- ❖ One or more Data and/or Special **Transmission Characters** may be grouped into **Transmission Words**.
- ❖ Special Transmission Words called **Ordered Sets** are defined.
- ❖ Ordered Sets are flexible building blocks which may be used for **in-band** or **out-of-band** protocol functions.



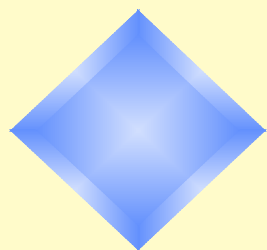
Ordered Set Usage

- ❖ Various coding objectives suggest the the specification of multiple length ordered sets.
 - A single character ordered set is required to ensure that the packet or carrier extension always ends on an odd-numbered character.
 - Multiple character ordered sets are required for sequences which include a comma and communicate a small amount of information. Two-character ordered sets provide 16/20 bit alignment.
 - The current requirements for automatic capability detection call for the communication of greater than 8 bits of information which requires either multiple 2 character sequences or the use of larger ordered sets. The use of 4 character ordered sets provides ample coding space and provides information within a single ordered set.
- ❖ Packets and sequences shall start only on even-numbered characters for consistency and error robustness.
 - This includes intermediate packets within a burst of packets.



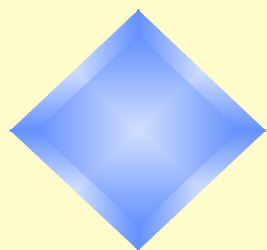
Special Character Usage

- ❖ The K28.5 special character is chosen as the first character of all sequences for the following reasons:
 - Bits abcdeif make up a comma. A comma is a singular bit pattern which in the absence of transmission errors cannot appear in any other location of a transmission character and cannot be generated across the boundaries of any two adjacent transmission characters.
 - The comma can be used to easily find and verify character and word boundaries of the received bit stream.
 - Bits ghj of the encoded character present the maximum number of transitions, simplifying receiver acquisition of bit synchronization.
- ❖ Special characters other than K28.5 are specified for single character ordered sets for alignment purposes or to provide timely function recognition.
 - Other special characters are chosen from the list of 12 available special characters.
 - The list is reduced to 9 when special characters containing a comma are excluded to prevent ordered set alignment on odd-numbered characters.



Defined Ordered Sets IDLE Sequence

- ❖ The I sequence is used to signal IDLE.
 - The I sequence effects the LINK UP primitive which indicates that the link is available to send packets.
 - The first I sequence following a packet or link configuration sequence shall restore the current positive or negative running disparity to a negative value. Two I sequence codes are required for this purpose.
 - All subsequent I sequences shall insure negative running disparity.
 - I sequences, including the first after a packet or link configuration sequence, shall be capable of signaling link DEFER/NOT DEFER status. Two additional I sequence codes are required for this purpose.
 - I codes should have a high transition density to keep the receiver in optimum sync during the high-frequency IDLE sequence.
 - A set of four I codes, I1, I2, I3 and I4, are defined consisting of a K28.5 special character followed by a data character.
 - Distinct carrier events should be separated by IDLEs. When a receiver sees any IDLE, it drops carrier.

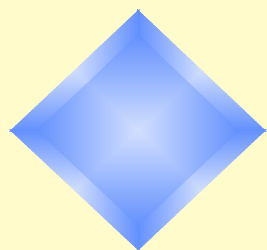


Defined Ordered Sets

Start and End of Packet Delimiters

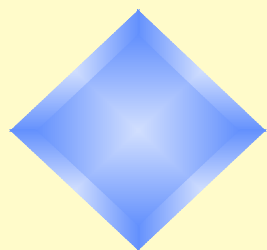
- ❖ The S delimiter is used to signal Start-Of-Packet (SOP).
 - A single character ordered set is desired in order to quickly assert the CSMA/CD carrier indication.
 - S follows IDLE for the first packet during a carrier event.
 - S follows R for subsequent packets during a carrier event.

- ❖ The T delimiter is used to signal End-Of-Packet (EOP).
 - A single character ordered set is desired in order to assist in quick de-assertion of the carrier indication.



Defined Ordered Sets Align/Extend Sequence

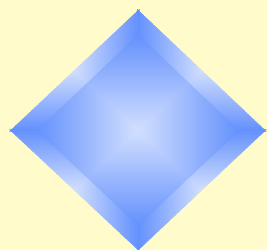
- ❖ The R signal is used to force even-numbered character alignment for the first IDLE following a carrier event and to extend the carrier following a packet when necessary.
 - A single character ordered set is required.
 - If T is transmitted as an odd-numbered character, and the carrier is not extended, T shall be followed by two successive R signals.
 - ◆ Two R's rather than none are required because of the possibility of running disparity error propagation to characters beyond those during which the error occurred.
 - If T is transmitted as an even-numbered character, and the carrier is not extended, exactly one R shall be transmitted after the T.
 - Additional R's shall be transmitted following a T to extend the carrier as required. The last R to extend the carrier must be transmitted in an odd-numbered character position.
- ❖ R shall also be used to separate the packets within a burst.



Defined Ordered Sets

Invalid Packet Delimiter/Signal

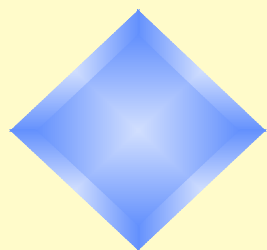
- ❖ The H delimiter and signal is used to replace individual invalid data and delimiters characters and mark those entities as invalid.
 - A single character ordered set is required.
 - An inter-station unit, such as a repeater, may substitute H for invalid data and delimiters upon detection of invalid characters.
 - H shall **not** be used to replace R.
 - ◆ The last H to extend the carrier must be transmitted in an odd-numbered character position.



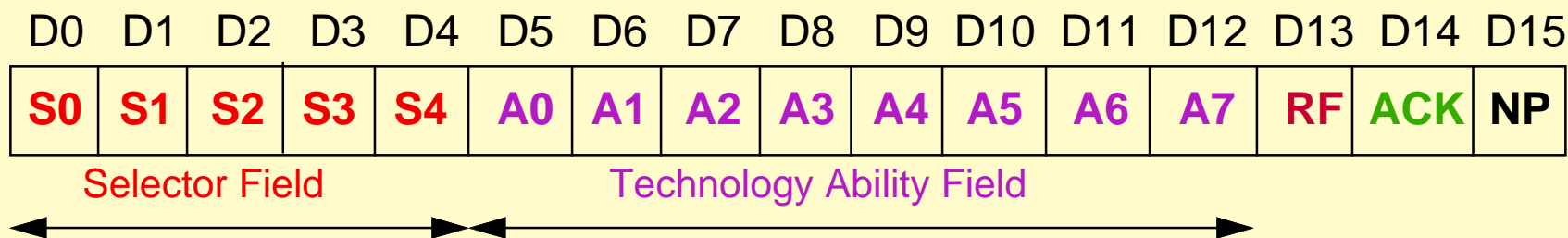
Defined Ordered Sets

LINK_NOT_AVAILABLE & LINK_CONFIGURATION

- ❖ The F sequence is used to indicate LINK_NOT_AVAILABLE.
 - The F sequence is signaled continuously while the associated receiver attempts to acquire synchronization.
- ❖ The C Sequence is used to indicate LINK_CONFIGURATION.
 - C conveys a single parameter to the other end of the link.
 - ◆ The parameter is a 16-bit config_register that includes bits sufficient to specify the capabilities of a PHY as well as an ACK bit.
 - ◆ Config_Register format is styled after the Link Code Word (LCW) defined in IEEE 802.3u clause 28.
 - Config_Register data bits are coded as the third and fourth characters of the LINK_CONFIGURATION ordered set.
 - The order of transmission of config_register data is encoded bits d0:d7 followed by encoded bits d8:d15.
 - ◆ The transmitted bit streams bears little resemblance to order of the Config_Register.

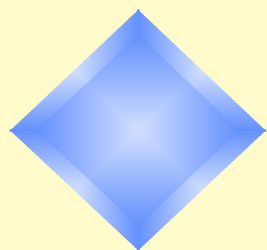


Config_Register



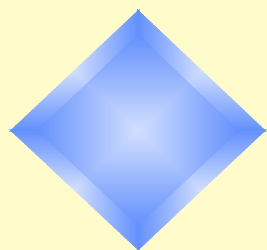
Config_Register bit usage:

- D5/A0: Full duplex capable
- D6/A1: Half duplex capable
- D7/A2: Defer capable
- D8/A3: Long Topology
- D9/A4: Short Topology
- D13/RF: Remote Fault
- D14/ACK: Acknowledge
- D15/NP: Next Page (Escape)



Listing of Ordered Sets

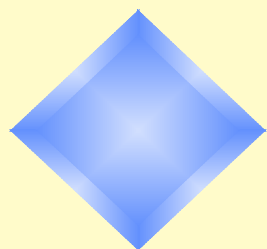
Code	Function	Encoding	Beg. RD	End RD
F	LINK_NOT_AVAILABLE	K28.5 D21.5	?	flip
C	LINK_CONFIGURATION	K28.5 D10.5 config_reg	?	?
I1	Flip Disparity/Not Defer	K28.5 D5.6	+	-
I2	Flip Disparity/Defer	K28.5 D26.1	+	-
I3	Disparity OK/Not Defer	K28.5 D16.2	-	-
I4	Disparity OK/Defer	K28.5 D2.2	-	-
S	SOP	K27.7	?	same
T	EOP1	K23.7	?	same
R	EOP2	K29.7	?	same
H	EOPinvalid	K30.7	?	same



Coding Distance of Characters Used in Ordered Sets

Char	D21.5	D2.2	D16.2	D10.5	D26.1
D2.2	7	↓	↓	↓	↓
D16.2	7	4	↓	↓	↓
D10.5	6	7	7	↓	↓
D26.1	6	3	5	4	↓
D5.6	4	7	4	6	10

- ❖ **Minimum** distance is 3, where, in both cases, the 3 bit positions are **not** successive.
- ❖ Data characters are chosen for high transition density, proper disparity control, and sufficient coding distance.



Link Information Example

Part 1/2

802.3 info

LINK_NOT_AVAILABLE
 LINK_NOT_AVAILABLE
 ~
 LINK_NOT_AVAILABLE
 LINK_CONFIGURATION
 LINK_CONFIGURATION
 ~
 LINK_CONFIGURATION
 Disparity OK/Not Defer
 Disparity OK/Not Defer
 ~
 Disparity OK/Not Defer
 0 PREAMBLE
 1 PREAMBLE
 2 PREAMBLE
 3 PREAMBLE
 4 PREAMBLE
 5 PREAMBLE
 6 PREAMBLE
 7 SFD
 8 DA
 ~
 LLC DATA
 ~
 FCS1

8B10B codes

F
 F
 ~
 F
 C
 C
 ~
 C
 I3
 I3
 ~
 I3
 S (single short packet)
 Data = 10101010
 Data = 10101010
 Data = 10101010
 Data = 10101010
 Data = 10101010
 Data = 10101010
 Data = 10101011
 Data = DA...
 ~
 Data = LLC DATA...
 ~
 Data = FCS1 octet...

802.3 info

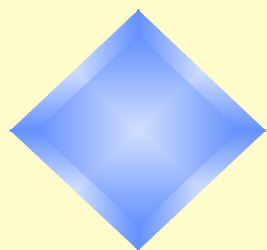
FCS2
 FCS3
 FCS4
 EOP1
 EOP2
 EOP2
 ~
 EOP2
 Flip Disparity/Not Defer
 Disparity OK/Not Defer
 ~
 Disparity OK/Not Defer
 Disparity OK/Defer
 Disparity OK/Defer
 ~
 Disparity OK/Defer
 Disparity OK/Not Defer
 LINK_NOT_AVAILABLE
 LINK_NOT_AVAILABLE
 ~
 LINK_NOT_AVAILABLE
 LINK_CONFIGURATION
 LINK_CONFIGURATION
 ~
 LINK_CONFIGURATION

8B10B codes

Data = FCS2 octet...
 Data = FCS3 octet...
 Data = FCS4 octet...
 T
 R
 R
 ~
 R (odd-num character)
 I1
 I3
 ~
 I3
 I4
 I4
 ~
 I4
 I3
 F (error detected)
 F
 ~
 F
 C
 C
 ~
 C

IEEE 802.3z

Gigabit Ethernet



Link Information Example

Part 2/2

802.3 info

Flip Disparity/Not Defer
 Disparity OK/Not Defer
 ~
 Disparity OK/Not Defer
 Disparity OK/Defer
 Disparity OK/Defer

0 PREAMBLE
 1 PREAMBLE
 2 PREAMBLE
 3 PREAMBLE
 4 PREAMBLE
 5 PREAMBLE
 6 PREAMBLE
 7 SFD
 8 DA

~
LLC DATA

~
 FCS1
 FCS2
 FCS3
 FCS4
 EOP1
 EOP2

8B10B codes

I1
 I3
 ~
 I3
 I4
 I4

S (1st packet of burst)

Data = 10101010
 Data = 10101010
 Data = 10101010
 Data = 10101010
 Data = 10101010
 Data = 10101010
 Data = 10101011
 Data = DA...

~
Data = LLC DATA...

~
 Data = FCS1 octet...
 Data = FCS2 octet...
 Data = FCS3 octet...
 Data = FCS4 octet...

T (even char/no extension)
 R

802.3 info

0 PREAMBLE
 1 PREAMBLE
 2 PREAMBLE
 3 PREAMBLE
 4 PREAMBLE
 5 PREAMBLE
 6 PREAMBLE
 7 SFD
 8 DA

~
LLC DATA

~
 FCS1
 FCS2
 FCS3
 FCS4
 EOP1
 EOP2

Flip Disparity/Defer
 Disparity OK/Defer

~
 Disparity OK/Defer
 Disparity OK/Not Defer
 Disparity OK/Not Defer

~

8B10B codes

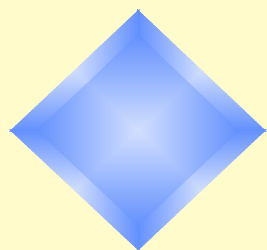
S (2nd packet of burst)
 Data = 10101010
 Data = 10101010
 Data = 10101010
 Data = 10101010
 Data = 10101010
 Data = 10101010
 Data = 10101011
 Data = DA...

~
Data = LLC DATA...

~
 Data = FCS1 octet...
 Data = FCS2 octet...
 Data = FCS3 octet...
 Data = FCS4 octet...

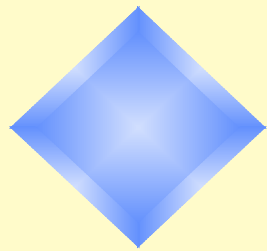
T (even char/no extension)

R
 I2
 I4
 ~
 I4
 I3
 I3
 ~



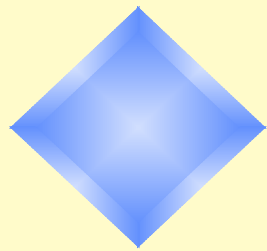
Link Initialization

- ❖ The link is not considered usable until Link Initialization is complete.
 - To perform link initialization, a station transmits a prescribed sequence and simultaneously attempts to acquire bit and transmission word synchronization from the received signal.
 - The sequence transmitted varies according to whether the link is initializing, has lost synchronization while initializing, or has completed initialization.
 - Link initialization may occur during the transmission of the LINK_NOT_AVAILABLE, LINK_CONFIGURATION, or IDLE sequences.



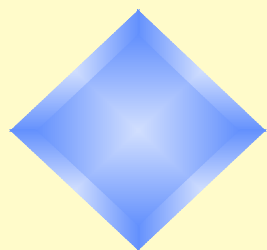
Invalid Transmission Words

- ❖ The detection of Invalid Transmission Words is an indication that a receiver is out of synchronization.
- ❖ An invalid Transmission Word is recognized by the receiver when one of the following conditions is detected:
 - A Code Violation is detected within a Transmission Word;
 - A Special Character Alignment Error is detected. (e.g., a K28.5 character is received as an odd-numbered character, a non-K28.5 special character immediately follows a K28.5 character, a non supported special character is detected, etc.);
 - An ordered set with improper Beginning Running Disparity received.



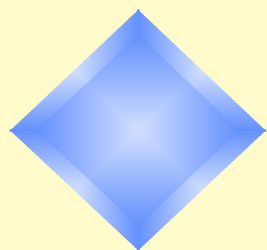
Running Disparity

- ❖ 8B10B code recognizes the idea of a Running Disparity (the difference between the number of 1's and 0's transmitted).
 - The sender keeps the running disparity around zero, the receiver checks the sender.
 - ◆ After powering on or exiting diagnostic mode, the transmitter assumes the negative value for its initial running disparity.
 - ◆ Upon transmission of any transmission character, the transmitter calculates a new value for its running disparity.
 - ◆ After powering on or exiting a special mode, the receiver assumes either a positive or negative initial running disparity.
 - ◆ Upon reception of any transmission character, the receiver determines whether the character is valid and calculates a new value for its RD.
 - ◆ All IDLE ordered sets end with negative RD. I3 and I4 ordered sets also begin with negative running disparity.
 - ◆ I3 or I4 ordered sets may be removed or added from an encoded bit stream by an inter-station unit to compensate for differences in clock frequencies, one word at a time, without altering the beginning RD of the immediately preceding transmission word.



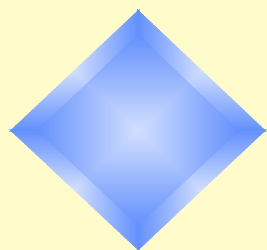
Synchronization States

- ❖ A receiver shall enter the **Synchronization_Acquired** state when it has achieved both bit and transmission word synchronization.
 - **Signal_status=OK** when a receiver is in the Synchronization_Acquired state.
- ❖ The following four conditions shall cause an operational receiver to enter the **Loss_of_Synchronization** state.
 - **Signal_status=NOT_OK** when a receiver is in the Loss_of_Synchronization state:
 - 1) Completion of the Loss_of_Synchronization procedure;
 - 2) Transition to power on;
 - 3) Exit from receiver reset condition;
 - 4) Detection of Loss_of_Signal.



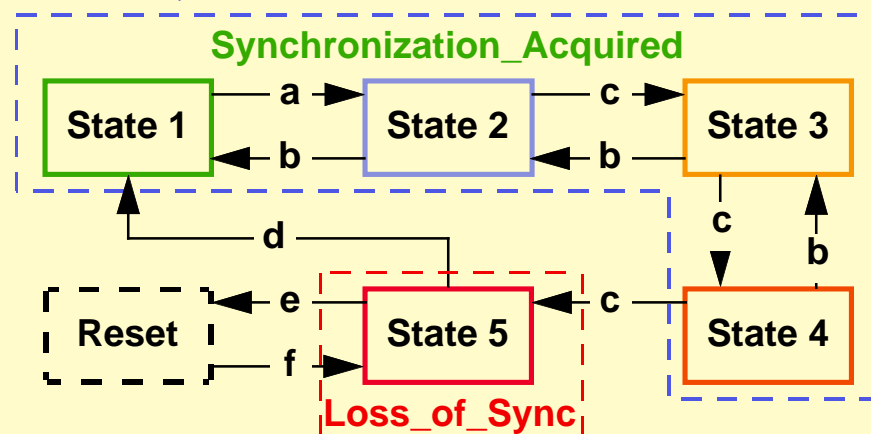
Loss_of_Synchronization Procedure States

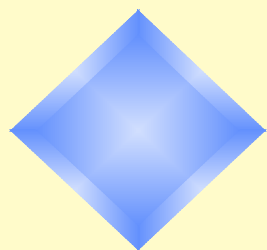
- ❖ The following five detection states are defined as part of the **Loss_of_Synchronization** procedure:
 - State 1: **No** invalid transmission word has been detected (the **No_Invalid_Transmission_Word** detection state).
 - State 2: The **first** invalid transmission word is detected (the **First_Invalid_Transmission_Word** detection state).
 - State 3: The **second** invalid transmission word is detected (the **Second_Invalid_Transmission_Word** detection state).
 - State 4: The **third** invalid transmission word is detected (the **Third_Invalid_Transmission_Word** detection state).
 - State 5: The **fourth** invalid transmission word is detected (the **Fourth_Invalid_Transmission_Word** detection state).
- ❖ A receiver in the **Synchronization_Acquired** state may be in any of the first four detection states listed above. A receiver in State 5 shall enter the **Loss_of_Synchronization** state.



Loss_of_Synchronization Procedure Transitions

- ❖ The following state transitions are defined as part of the Loss_of_Synchronization procedure:
 - a) The first invalid transmission word is detected;
 - b) An additional invalid transmission word is not detected in the next two or fewer consecutive transmission words;
 - c) An additional invalid transmission word is detected in the next two or fewer consecutive transmission words;
 - d) The receiver regains synchronization;
 - e) The receiver is reset;
 - f) The receiver exits a previously established reset condition.





Summary

- ❖ 8B10B codes and the proposed coding structure is efficient, robust, and flexible enough to meet Gigabit Ethernet PCS requirements.
- ❖ Follow-up activities:
 - Review Howard Johnson's Proof of Robustness
 - Maintenance mode protocol and coding
 - Reserved codes
 - Other direction from the Task Force?

Table 1 – Valid data characters

Data Byte Name	Bits HGF EDCBA	Current RD –	RD –	Current RD +	RD +	Combined Transition Density	Ending RD
		abcdei fghj	Transition Density	abcdei fghj	Transition Density		
D0.0	000 00000	100111 0100	5	011000 1011	5	10	same
D1.0	000 00001	011101 0100	6	100010 1011	6	12	same
D2.0	000 00010	101101 0100	7	010010 1011	7	14	same
D3.0	000 00011	110001 1011	4	110001 0100	5	9	flip
D4.0	000 00100	110101 0100	7	001010 1011	7	14	same
D5.0	000 00101	101001 1011	6	101001 0100	7	13	flip
D6.0	000 00110	011001 1011	5	011001 0100	6	11	flip
D7.0	000 00111	111000 1011	4	000111 0100	4	8	flip
D8.0	000 01000	111001 0100	5	000110 1011	5	10	same
D9.0	000 01001	100101 1011	6	100101 0100	7	13	flip
D10.0	000 01010	010101 1011	7	010101 0100	8	15	flip
D11.0	000 01011	110100 1011	6	110100 0100	5	11	flip
D12.0	000 01100	001101 1011	5	001101 0100	6	11	flip
D13.0	000 01101	101100 1011	6	101100 0100	5	11	flip
D14.0	000 01110	011100 1011	5	011100 0100	4	9	flip
D15.0	000 01111	010111 0100	6	101000 1011	6	12	same
D16.0	000 10000	011011 0100	6	100100 1011	6	12	same
D17.0	000 10001	100011 1011	4	100011 0100	5	9	flip
D18.0	000 10010	010011 1011	5	010011 0100	6	11	flip
D19.0	000 10011	110010 1011	6	110010 0100	5	11	flip
D20.0	000 10100	001011 1011	5	001011 0100	6	11	flip
D21.0	000 10101	101010 1011	8	101010 0100	7	15	flip
D22.0	000 10110	011010 1011	7	011010 0100	6	13	flip
D23.0	000 10111	111010 0100	5	000101 1011	5	10	same
D24.0	000 11000	110011 0100	5	001100 1011	5	10	same
D25.0	000 11001	100110 1011	6	100110 0100	5	11	flip
D26.0	000 11010	010110 1011	7	010110 0100	6	13	flip
D27.0	000 11011	110110 0100	5	001001 1011	5	10	same
D28.0	000 11100	001110 1011	5	001110 0100	4	9	flip
D29.0	000 11101	101110 0100	5	010001 1011	5	10	same
D30.0	000 11110	011110 0100	4	100001 1011	4	8	same
D31.0	000 11111	101011 0100	7	010100 1011	7	14	same
D0.1	001 00000	100111 1001	4	011000 1001	5	9	flip
D1.1	001 00001	011101 1001	5	100010 1001	6	11	flip
D2.1	001 00010	101101 1001	6	010010 1001	7	13	flip
D3.1	001 00011	110001 1001	4	110001 1001	4	8	same
D4.1	001 00100	110101 1001	6	001010 1001	7	13	flip
D5.1	001 00101	101001 1001	6	101001 1001	6	12	same
D6.1	001 00110	011001 1001	5	011001 1001	5	10	same
D7.1	001 00111	111000 1001	4	000111 1001	3	7	same
D8.1	001 01000	111001 1001	4	000110 1001	5	9	flip
D9.1	001 01001	100101 1001	6	100101 1001	6	12	same
D10.1	001 01010	010101 1001	7	010101 1001	7	14	same
D11.1	001 01011	110100 1001	6	110100 1001	6	12	same
D12.1	001 01100	001101 1001	5	001101 1001	5	10	same
D13.1	001 01101	101100 1001	5	101100 1001	5	10	same
D14.1	001 01110	011100 1001	5	011100 1001	5	10	same
D15.1	001 01111	010111 1001	5	101000 1001	6	11	flip
D16.1	001 10000	011011 1001	5	100100 1001	6	11	flip
D17.1	001 10001	100011 1001	4	100011 1001	4	8	same
D18.1	001 10010	010011 1001	5	010011 1001	5	10	same
D19.1	001 10011	110010 1001	6	110010 1001	6	12	same
D20.1	001 10100	001011 1001	5	001011 1001	5	10	same
D21.1	001 10101	101010 1001	8	101010 1001	8	16	same
D22.1	001 10110	011010 1001	7	011010 1001	7	14	same
D23.1	001 10111	111010 1001	6	000101 1001	5	11	flip
D24.1	001 11000	110011 1001	4	001100 1001	5	9	flip
D25.1	001 11001	100110 1001	6	100110 1001	6	12	same
D26.1	001 11010	010110 1001	7	010110 1001	7	14	same
D27.1	001 11011	110110 1001	6	001001 1001	5	11	flip

(continued)

Table 1 – Valid data characters (*continued*)

Data Byte Name	Bits HGF EDCBA	Current RD –	RD –	Current RD +	RD +	Combined Transition Density	Ending RD
		abcdei fghj	Transition Density	abcdei fghj	Transition Density		
D28.1	001 11100	001110 1001	5	001110 1001	5	10	same
D29.1	001 11101	101110 1001	6	010001 1001	5	11	flip
D30.1	001 11110	011110 1001	5	100001 1001	4	9	flip
D31.1	001 11111	101011 1001	6	010100 1001	7	13	flip
D0.2	010 00000	100111 0101	6	011000 0101	5	11	same
D1.2	010 00001	011101 0101	7	100010 0101	6	13	flip
D2.2	010 00010	101101 0101	8	010010 0101	7	15	flip
D3.2	010 00011	110001 0101	6	110001 0101	6	12	same
D4.2	010 00100	110101 0101	8	001010 0101	7	15	flip
D5.2	010 00101	101001 0101	8	101001 0101	8	16	same
D6.2	010 00110	011001 0101	7	011001 0101	7	14	same
D7.2	010 00111	111000 0101	4	000111 0101	5	9	same
D8.2	010 01000	111001 0101	6	000110 0101	5	11	flip
D9.2	010 01001	100101 0101	8	100101 0101	8	16	same
D10.2	010 01010	010101 0101	9	010101 0101	9	18	same
D11.2	010 01011	110100 0101	6	110100 0101	6	12	same
D12.2	010 01100	001101 0101	7	001101 0101	7	14	same
D13.2	010 01101	101100 0101	6	101100 0101	6	12	same
D14.2	010 01110	011100 0101	5	011100 0101	5	10	same
D15.2	010 01111	010111 0101	7	101000 0101	6	13	flip
D16.2	010 10000	011011 0101	7	100100 0101	6	13	flip
D17.2	010 10001	100011 0101	6	100011 0101	6	12	same
D18.2	010 10010	010011 0101	7	010011 0101	7	14	same
D19.2	010 10011	110010 0101	6	110010 0101	6	12	same
D20.2	010 10100	001011 0101	7	001011 0101	7	14	same
D21.2	010 10101	101010 0101	8	101010 0101	8	16	same
D22.2	010 10110	011010 0101	7	110101 0101	7	14	same
D23.2	010 10111	111010 0101	6	000101 0101	7	13	flip
D24.2	010 11000	110011 0101	6	001100 0101	5	11	flip
D25.2	010 11001	100110 0101	6	100110 0101	6	12	same
D26.2	010 11010	010110 0101	7	010110 0101	7	14	same
D27.2	010 11011	110110 0101	6	001001 0101	7	13	flip
D28.2	010 11100	001110 0101	5	001110 0101	5	10	same
D29.2	010 11101	101110 0101	6	010001 0101	7	13	flip
D30.2	010 11110	011110 0101	5	100001 0101	6	11	flip
D31.2	010 11111	101011 0101	8	010100 0101	7	15	flip
D0.3	011 00000	100111 0011	4	011000 1100	4	8	flip
D1.3	011 00001	011101 0011	5	100010 1100	5	10	flip
D2.3	011 00010	101101 0011	6	010010 1100	6	12	flip
D3.3	011 00011	110001 1100	3	110001 0011	4	7	same
D4.3	011 00100	110101 0011	6	001010 1100	6	12	flip
D5.3	011 00101	101001 1100	5	101001 0011	6	11	same
D6.3	011 00110	011001 1100	4	011001 0011	5	9	same
D7.3	011 00111	111000 1100	3	000111 0011	3	6	same
D8.3	011 01000	111001 0011	4	000110 1100	4	8	flip
D9.3	011 01001	100101 1100	5	100101 0011	6	11	same
D10.3	011 01010	010101 1100	6	010101 0011	7	13	same
D11.3	011 01011	110100 1100	5	110100 0011	4	9	same
D12.3	011 01100	001101 1100	4	001101 0011	5	9	same
D13.3	011 01101	101100 1100	5	101100 0011	4	9	same
D14.3	011 01110	011100 1100	4	011100 0011	3	7	same
D15.3	011 01111	010111 0011	5	101000 1100	5	10	flip
D16.3	011 10000	011011 0011	5	100100 1100	5	10	flip
D17.3	011 10001	100011 1100	3	100011 0011	4	7	same
D18.3	011 10010	010011 1100	4	010011 0011	5	9	same
D19.3	011 10011	110010 1100	5	110010 0011	4	9	same
D20.3	011 10100	001011 1100	4	001011 0011	5	9	same
D21.3	011 10101	101010 1100	7	101010 0011	6	13	same
D22.3	011 10110	011010 1100	6	011010 0011	5	11	same
D23.3	011 10111	111010 0011	4	000101 1100	4	8	flip

(continued)

Table 1 – Valid data characters (continued)

Data Byte Name	Bits HGF EDCBA	Current RD –	RD –	Current RD +	RD +	Combined Transition Density	Ending RD
		abcdei fghj	Transition Density	abcdei fghj	Transition Density		
D24.3	011 11000	110011 0011	4	001100 1100	4	8	flip
D25.3	011 11001	100110 1100	5	100110 0011	4	9	same
D26.3	011 11010	010110 1100	6	010110 0011	5	11	same
D27.3	011 11011	110110 0011	4	001001 1100	4	8	flip
D28.3	011 11100	001110 1100	4	001110 0011	3	7	same
D29.3	011 11101	101110 0011	4	010001 1100	4	8	flip
D30.3	011 11110	011110 0011	3	100001 1100	3	6	flip
D31.3	011 11111	101011 0011	6	010100 1100	6	11	flip
D0.4	100 00000	100111 0010	5	011000 1101	5	10	same
D1.4	100 00001	011101 0010	6	100010 1101	6	12	same
D2.4	100 00010	101101 0010	7	010010 1101	7	14	same
D3.4	100 00011	110001 1101	4	110001 0010	5	9	flip
D4.4	100 00100	110101 0010	7	001010 1101	7	14	same
D5.4	100 00101	101001 1101	6	101001 0010	7	13	flip
D6.4	100 00110	011001 1101	5	011001 0010	6	11	flip
D7.4	100 00111	111000 1101	4	000111 0010	4	8	flip
D8.4	100 01000	111001 0010	5	000110 1101	5	10	same
D9.4	100 01001	100101 1101	6	100101 0010	7	13	flip
D10.4	100 01010	010101 1101	7	010101 0010	8	15	flip
D11.4	100 01011	110100 1101	6	110100 0010	5	11	flip
D12.4	100 01100	001101 1101	5	001101 0010	6	11	flip
D13.4	100 01101	101100 1101	6	101100 0010	5	11	flip
D14.4	100 01110	011100 1101	5	011100 0010	4	9	flip
D15.4	100 01111	010111 0010	6	101000 1101	6	12	same
D16.4	100 10000	011011 0010	6	100100 1101	6	12	same
D17.4	100 10001	100011 1101	4	100011 0010	5	9	flip
D18.4	100 10010	010011 1101	5	010011 0010	6	11	flip
D19.4	100 10011	110010 1101	6	110010 0010	5	11	flip
D20.4	100 10100	001011 1101	5	001011 0010	6	11	flip
D21.4	100 10101	101010 1101	8	101010 0010	7	15	flip
D22.4	100 10110	011010 1101	7	011010 0010	6	13	flip
D23.4	100 10111	111010 0010	5	000101 1101	5	10	same
D24.4	100 11000	110011 0010	5	001100 1101	5	10	same
D25.4	100 11001	100110 1101	6	100110 0010	5	11	flip
D26.4	100 11010	010110 1101	7	010110 0010	6	13	flip
D27.4	100 11011	110110 0010	5	001001 1101	5	10	same
D28.4	100 11100	001110 1101	5	001110 0010	4	9	flip
D29.4	100 11101	101110 0010	5	010001 1101	5	10	same
D30.4	100 11110	011110 0010	4	100001 1101	4	8	same
D31.4	100 11111	101011 0010	7	010100 1101	7	14	same
D0.5	101 00000	100111 1010	5	011000 1010	6	11	flip
D1.5	101 00001	011101 1010	6	100010 1010	7	13	flip
D2.5	101 00010	101101 1010	7	010010 1010	8	15	flip
D3.5	101 00011	110001 1010	5	110001 1010	5	10	same
D4.5	101 00100	110101 1010	7	001010 1010	8	15	flip
D5.5	101 00101	101001 1010	7	101001 1010	7	14	same
D6.5	101 00110	011001 1010	6	011001 1010	6	12	same
D7.5	101 00111	111000 1010	5	000111 1010	4	9	same
D8.5	101 01000	111001 1010	5	000110 1010	6	11	flip
D9.5	101 01001	100101 1010	7	100101 1010	7	14	same
D10.5	101 01010	010101 1010	8	010101 1010	8	16	same
D11.5	101 01011	110100 1010	7	110100 1010	7	14	same
D12.5	101 01100	001101 1010	6	001101 1010	6	12	same
D13.5	101 01101	101100 1010	7	101100 1010	7	14	same
D14.5	101 01110	011100 1010	6	011100 1010	6	12	same
D15.5	101 01111	010111 1010	6	101000 1010	7	13	flip
D16.5	101 10000	011011 1010	6	100100 1010	7	13	flip
D17.5	101 10001	100011 1010	5	100011 1010	5	10	same
D18.5	101 10010	010011 1010	6	010011 1010	6	12	same
D19.5	101 10011	110010 1010	7	110010 1010	7	14	same

(continued)

Table 1 – Valid data characters (*continued*)

Data Byte Name	Bits HGF EDCBA	Current RD –	RD –	Current RD +	RD +	Combined Transition Density	Ending RD
		abcdei fghj	Transition Density	abcdei fghj	Transition Density		
D20.5	101 10100	001011 1010	6	001011 1010	6	12	same
D21.5	101 10101	101010 1010	9	101010 1010	9	18	same
D22.5	101 10110	011010 1010	8	011010 1010	8	16	same
D23.5	101 10111	111010 1010	7	000101 1010	6	13	flip
D24.5	101 11000	110011 1010	5	001100 1010	6	11	flip
D25.5	101 11001	100110 1010	7	100110 1010	7	14	same
D26.5	101 11010	010110 1010	8	010110 1010	8	16	same
D27.5	101 11011	110110 1010	7	001001 1010	6	13	flip
D28.5	101 11100	001110 1010	6	001110 1010	6	12	same
D29.5	101 11101	101110 1010	7	010001 1010	6	13	flip
D30.5	101 11110	011110 1010	6	100001 1010	5	11	flip
D31.5	101 11111	101011 1010	7	010100 1010	8	15	flip
D0.6	110 00000	100111 0110	5	011000 0110	4	9	flip
D1.6	110 00001	011101 0110	6	100010 0110	5	11	flip
D2.6	110 00010	101101 0110	7	010010 0110	6	13	flip
D3.6	110 00011	110001 0110	5	110001 0110	5	10	same
D4.6	110 00100	110101 0110	7	001010 0110	6	13	flip
D5.6	110 00101	101001 0110	7	101001 0110	7	14	same
D6.6	110 00110	011001 0110	6	011001 0110	6	12	same
D7.6	110 00111	111000 0110	3	000111 0110	4	7	same
D8.6	110 01000	111001 0110	5	000110 0110	4	9	flip
D9.6	110 01001	100101 0110	7	100101 0110	7	14	same
D10.6	110 01010	010101 0110	8	010101 0110	8	16	same
D11.6	110 01011	110100 0110	5	110100 0110	5	10	same
D12.6	110 01100	001101 0110	6	001101 0110	6	12	same
D13.6	110 01101	101100 0110	5	101100 0110	5	10	same
D14.6	110 01110	011100 0110	4	011100 0110	4	8	same
D15.6	110 01111	010111 0110	6	101000 0110	5	11	flip
D16.6	110 10000	011011 0110	6	100100 0110	5	11	flip
D17.6	110 10001	100011 0110	5	100011 0110	5	10	same
D18.6	110 10010	010011 0110	6	010011 0110	6	12	same
D19.6	110 10011	110010 0110	5	110010 0110	5	10	same
D20.6	110 10100	001011 0110	6	001011 0110	6	12	same
D21.6	110 10101	101010 0110	7	101010 0110	7	14	same
D22.6	110 10110	011010 0110	6	011010 0110	6	12	same
D23.6	110 10111	111010 0110	5	000101 0110	6	11	flip
D24.6	110 11000	110011 0110	5	001100 0110	4	9	same
D25.6	110 11001	100110 0110	5	100110 0110	5	10	same
D26.6	110 11010	010110 0110	6	010110 0110	6	12	same
D27.6	110 11011	110110 0110	5	001001 0110	6	11	flip
D28.6	110 11100	001110 0110	4	001110 0110	4	8	same
D29.6	110 11101	101110 0110	5	010001 0110	5	10	flip
D30.6	110 11110	011110 0110	4	100001 0110	5	9	flip
D31.6	110 11111	101011 0110	7	010100 0110	6	13	flip
D0.7	111 00000	100111 0001	4	011000 1110	4	8	same
D1.7	111 00001	011101 0001	5	100010 1110	5	10	same
D2.7	111 00010	101101 0001	6	010010 1110	6	12	same
D3.7	111 00011	110001 1110	3	110001 0001	4	7	flip[
D4.7	111 00100	110101 0001	5	001010 1110	6	11	same
D5.7	111 00101	101001 1110	5	101001 0001	6	11	flip
D6.7	111 00110	011001 1110	4	011001 0001	5	9	flip
D7.7	111 00111	111000 1110	3	000111 0001	3	6	flip
D8.7	111 01000	111001 0001	4	000110 1110	4	8	same
D9.7	111 01001	100101 1110	5	100101 0001	6	11	flip
D10.7	111 01010	010101 1110	6	010101 0001	7	13	flip
D11.7	111 01011	110100 1110	5	110100 1000	5	10	flip
D12.7	111 01100	001101 1110	4	001101 0001	5	9	flip
D13.7	111 01101	101100 1110	5	101100 1000	5	10	flip
D14.7	111 01110	011100 1110	4	011100 1000	4	8	flip
D15.7	111 01111	010111 0001	5	101000 1110	5	10	same

(continued)

Table 1 – Valid data characters (*continued*)

Data Byte Name	Bits HGF EDCBA	Current RD –	RD – Transition Density	Current RD +	RD + Transition Density	Combined Transition Density	Ending RD
		abcdei fghj		abcdei fghj			
D16.7	111 10000	011011 0001	5	100100 1110	5	10	same
D17.7	111 10001	100011 0111	4	100011 0001	4	8	flip
D18.7	111 10010	010011 0111	5	010011 0001	5	10	flip
D19.7	111 10011	110010 1110	5	110010 0001	4	9	flip
D20.7	111 10100	001011 0111	5	001011 0001	5	10	flip
D21.7	111 10101	101010 1110	7	101010 0001	6	13	flip
D22.7	111 10110	011010 1110	6	011010 0001	5	11	flip
D23.7	111 10111	111010 0001	4	000101 1110	4	8	same
D24.7	111 11000	110011 0001	4	001100 1110	4	8	same
D25.7	111 11001	100110 1110	5	100110 0001	4	9	flip
D26.7	111 11010	010110 1110	6	010110 0001	5	11	flip
D27.7	111 11011	110110 0001	4	001001 1110	4	8	same
D28.7	111 11100	001110 1110	4	001110 0001	3	7	flip
D29.7	111 11101	101110 0001	4	010001 1110	4	8	same
D30.7	111 11110	011110 0001	3	100001 1110	3	6	same
D31.7	111 11111	101011 0001	6	010100 1110	6	12	same
<i>(concluded)</i>							

Table 12 – Valid special characters

Special Code Name	Current RD –	Current RD +	Notes	Ending RD
	abcdei fghj	abcdei fghj		
K28.0	001111 0100	110000 1011	Comma	same
K28.1	001111 1001	110000 0110		flip
K28.2	001111 0101	110000 1010	Comma	flip
K28.3	001111 0011	110000 1100		flip
K28.4	001111 0010	110000 1101	Comma	same
K28.5	001111 1010	110000 0101		flip
K28.6	001111 0110	110000 1001	Comma	flip
K28.7	001111 1000	110000 0111		same
K23.7	111010 1000	000101 0111		same
K27.7	110110 1000	001001 0111		same
K29.7	101110 1000	010001 0111		same
K30.7	011110 1000	100001 0111		same
Notes				
Comma - comma character				