Performance of SONY 1.25Gbaud Transceiver IC (CXB1584Q)

1. Features of CXB1584Q

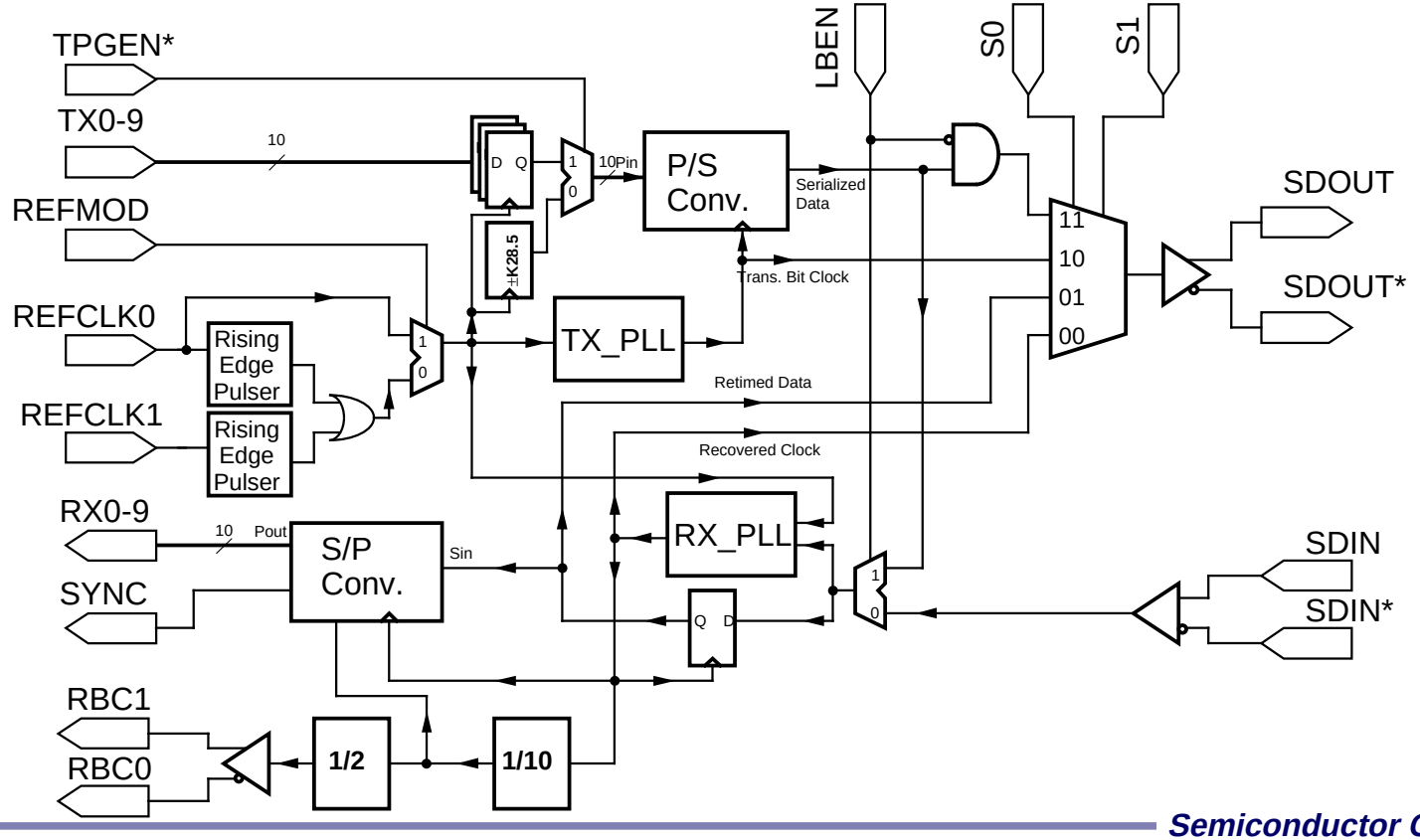
2. Performance comparison between 1.25Gbaud &1.06Gbaud
   (Conventional single reference clock operation)

3. New proposal of Half rate Dual Reference Clock Operation
   - Explanation about the operation
   - Performance
   - Dual Clock Skew Influence on the jitter characteristics

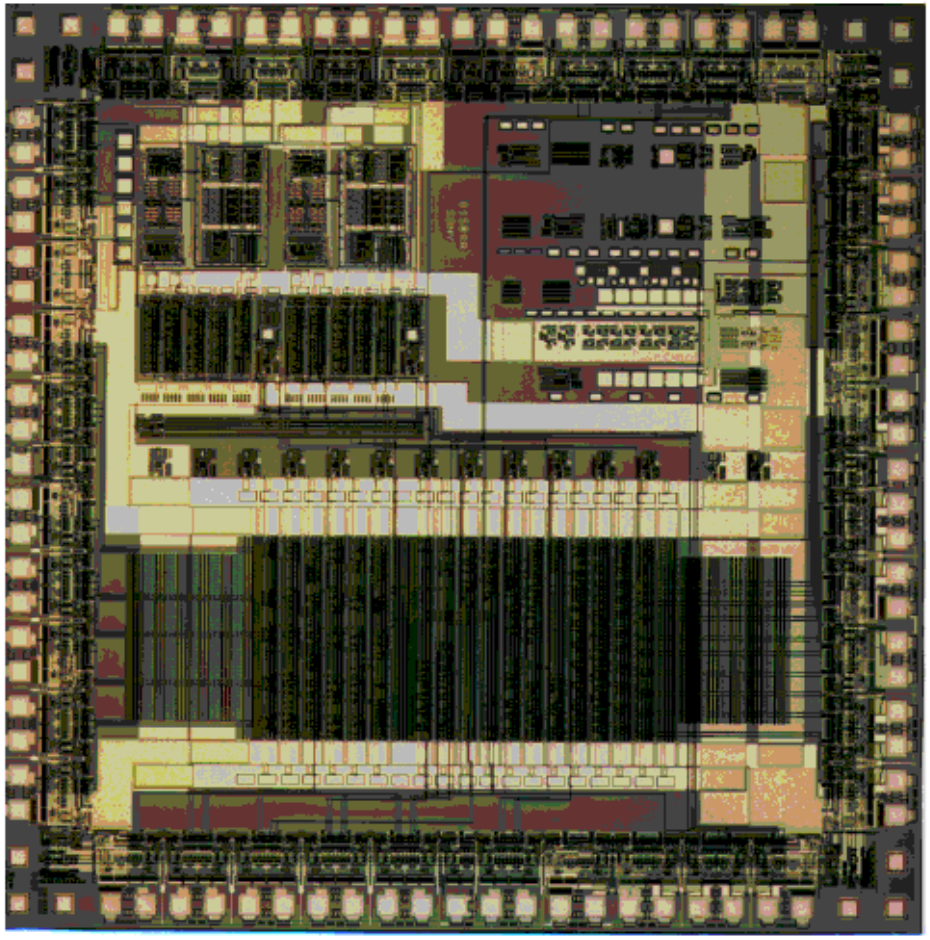
4. Conclusion

Features of CXB1584Q

- Test Chip for Gigabit ether Transceiver
- Fibre Channel compatible (FC_0) at 1.0625Gbaud
- On chip byte sync detector (+Comma)
- ***Selectable Single Reference Clock or Half rate Dual Reference Clocks***
- Lock detectors of Tx & Rx
- High speed data output selector (Transmit Data / Clock, Recovery Data / Clock)
- 3.3V single power supply
- 80pin Plastic QFP package (14mm x 14mm)
- Bit rate over 1.25GBaud
- On chip PLL for Tx & Rx
- On chip ±K28.5 pattern generator
- Built-in local loop back circuitry
- Low Power consumption (1W typical)



CXB1584Q Chip micrograph

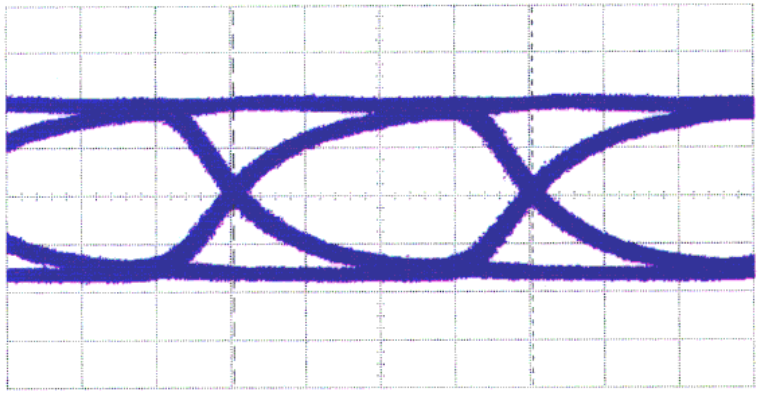


Chip Size : 4.98mm x 4.98mm
Process : 0.8um rule
Double poly Si Em/Base Self-aligned Bipolar
ft = 15GHz @Ic = 200uA, VCE = 3.0V

CXB1584Q TX Characteristics on Single REFCLK operation

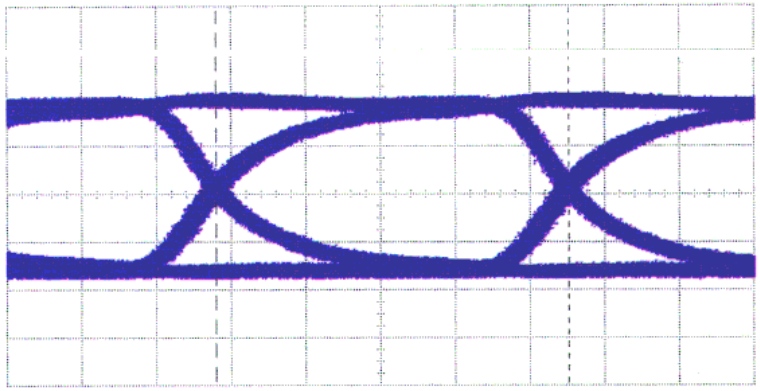
EYE PATTERN

Serial Data output at 1.25G baud



Time base : 200 ps/div
Vertical axis : 200 mV/div

Serial Data output at 1.06G baud

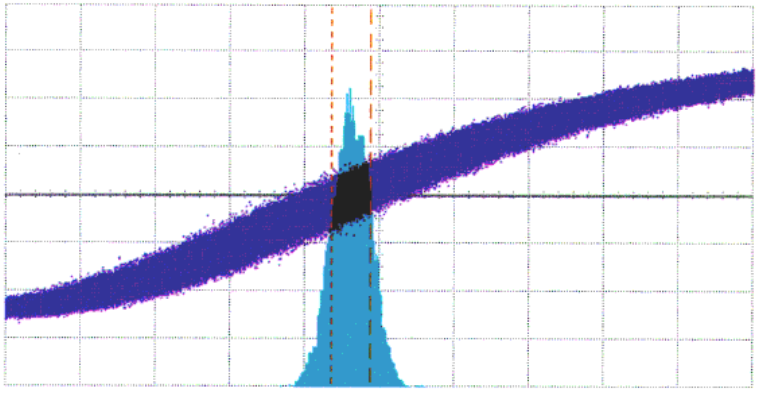


Time base : 200 ps/div
Vertical axis : 200 mV/div

CXB1584Q TX Characteristics on Single REFCLK operation

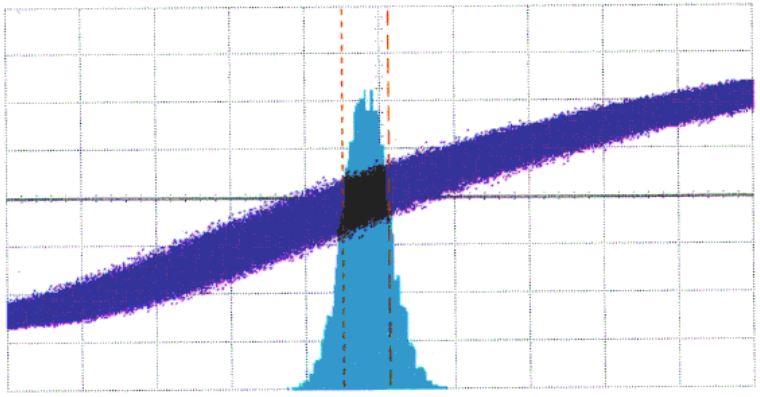
Random Jitter

Transmit bit clock at 1.25GHz
RJ(14σ)=107.8ps=0.135UI



Time base : 30 ps/div
Vertical axis : 100 mV/div
σ=7.7ps

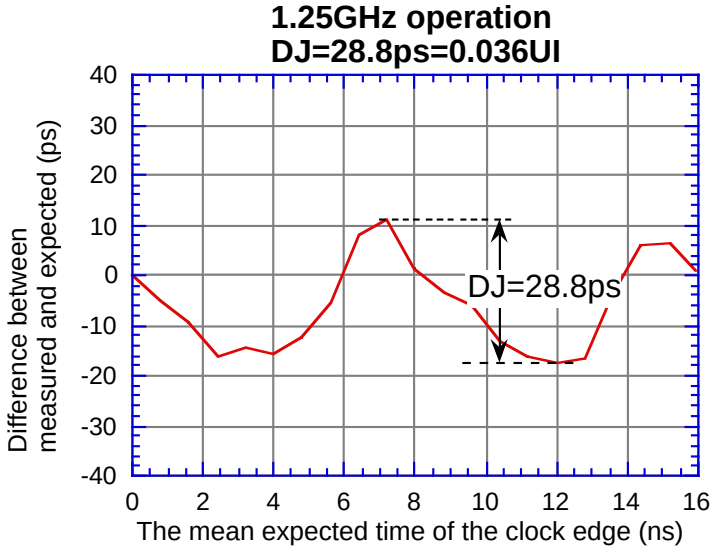
Transmit bit clock at 1.06GHz
RJ(14σ)=128.8ps=0.137UI

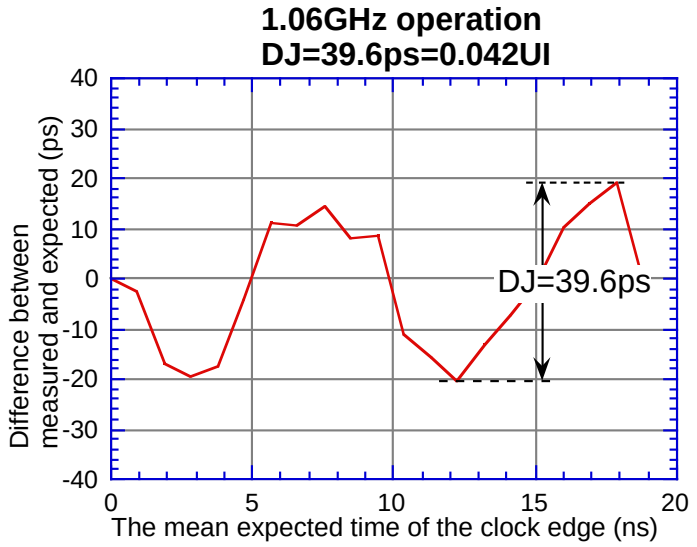


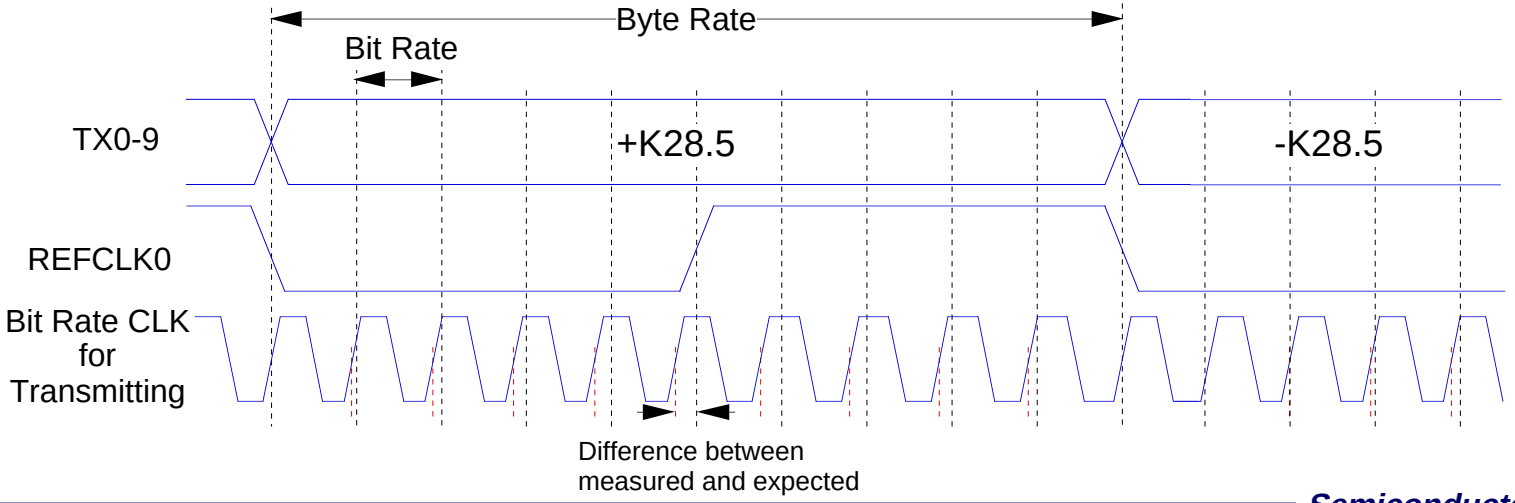
Time base : 30 ps/div
Vertical axis : 100 mV/div
σ=9.2ps

CXB1584Q TX Characteristics on Single REFCLK operation

DJ Measurement of Transmit bit clock

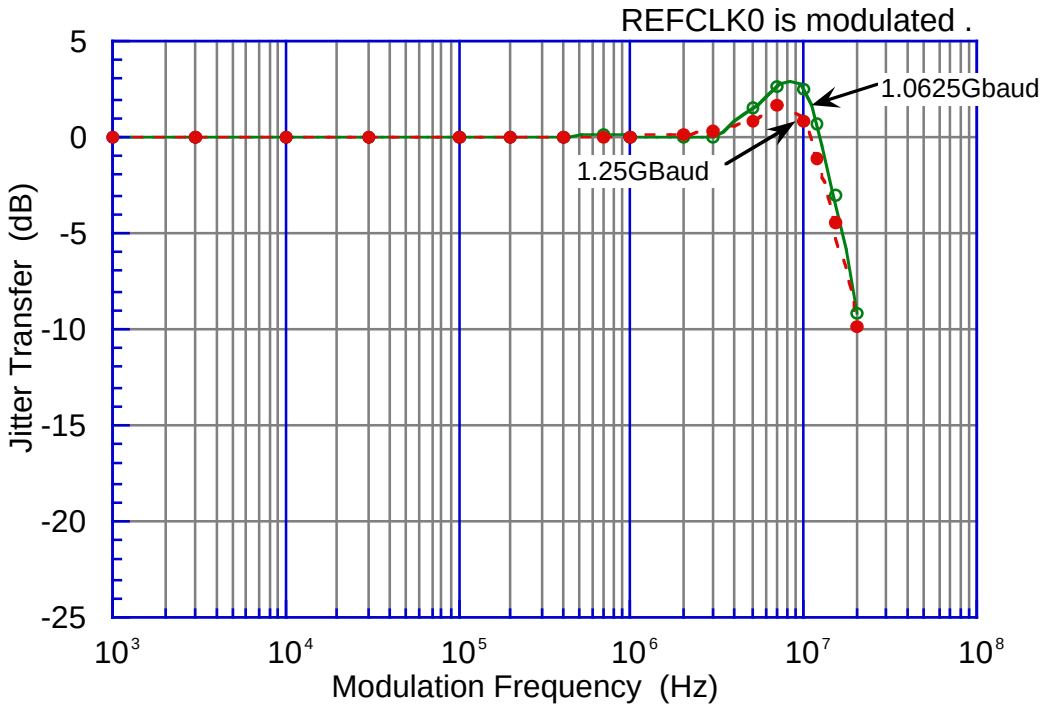


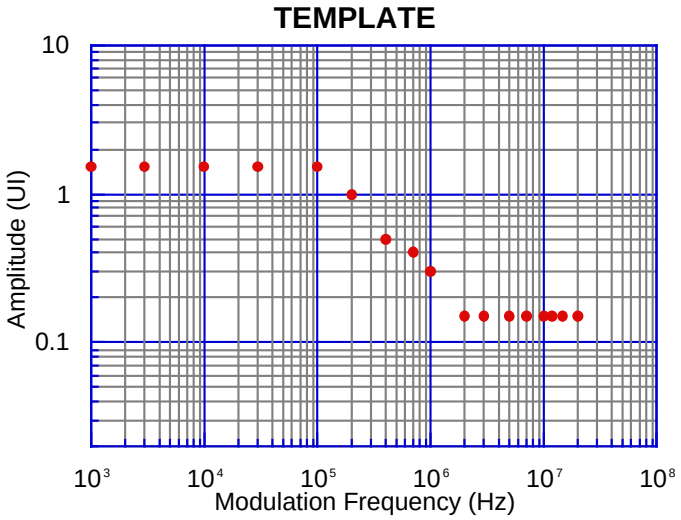




CXB1584Q TX Characteristics on Single REFCLK operation

TX Jitter Transfer

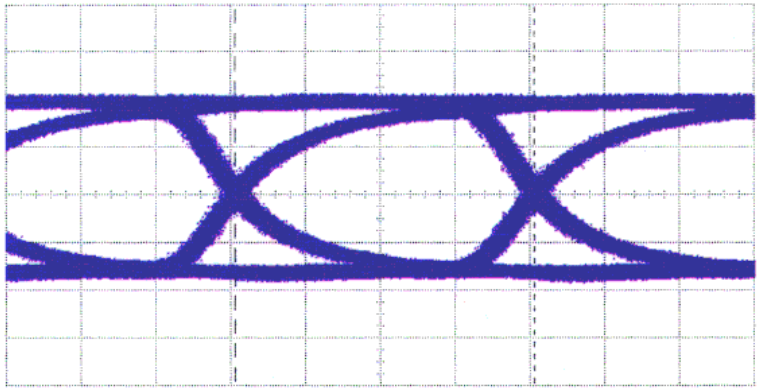




CXB1584Q RX Characteristics on Single REFCLK operation

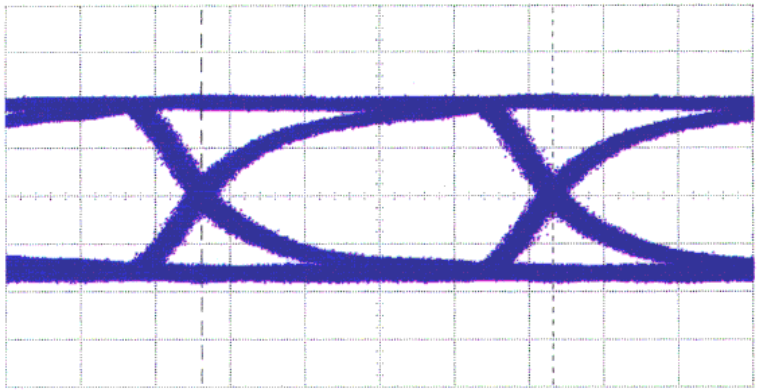
EYE PATTERN

Retimed Data at 1.25G baud



Time base : 200 ps/div
Vertical axis : 200 mV/div

Retimed Data at 1.06G baud



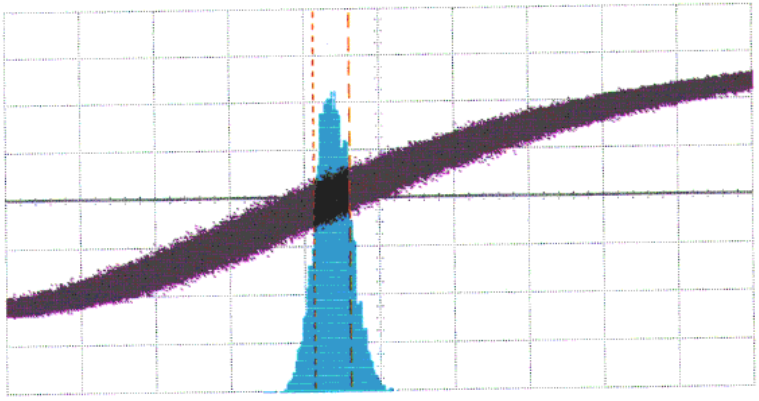
Time base : 200 ps/div
Vertical axis : 200 mV/div

CXB1584Q RX Characteristics on Single REFCLK operation

Random Jitter

Recovery clock at 1.25GHz
RJ(14σ)=98.0ps=0.123UI

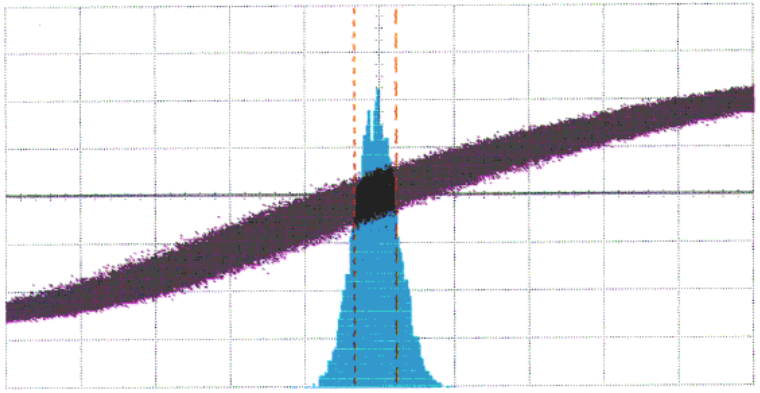
Serial Data : FC Idle (T.D.=80%)



Time base : 30 ps/div
Vertical axis : 100 mV/div
σ=7.0 ps

Recovery clock at 1.06GHz
RJ(14σ)=120.4ps=0.128UI

Serial Data : FC Idle (T.D.=80%)

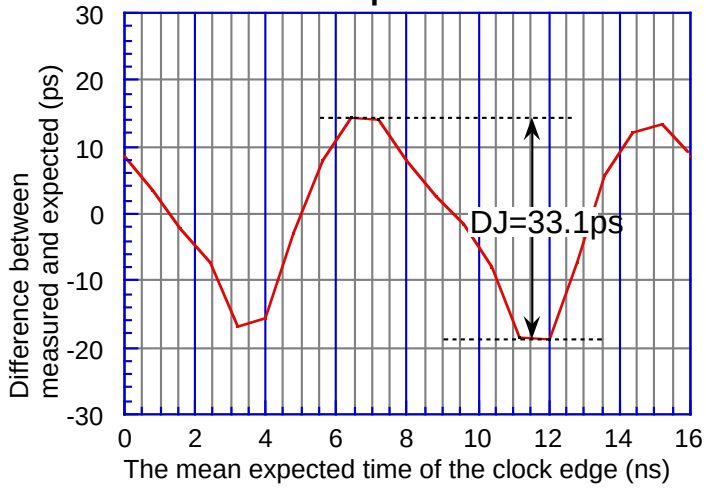


Time base : 30 ps/div
Vertical axis : 100 mV/div
σ=8.6 ps

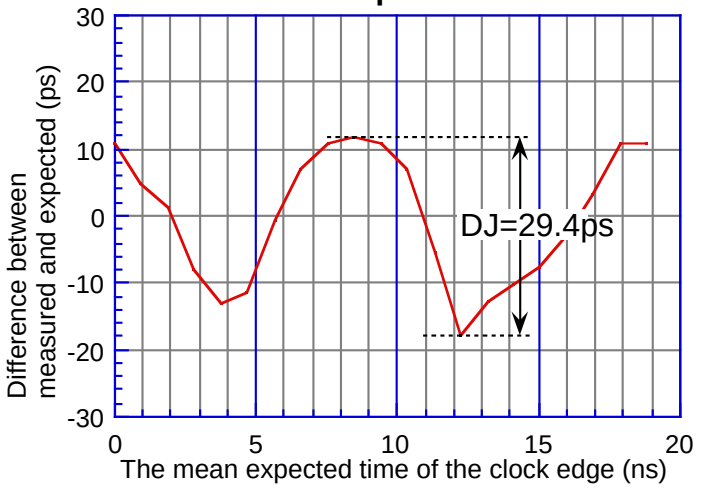
CXB1584Q RX Characteristics on Single REFCLK operation

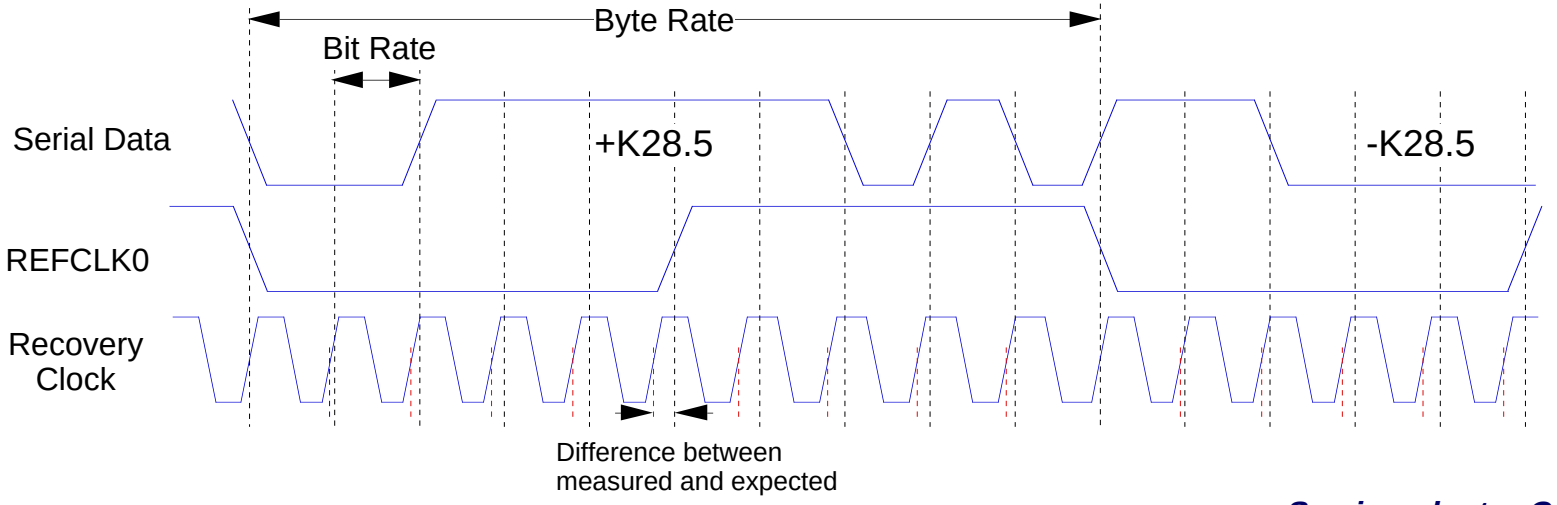
DJ Measurement of Recovery clock

1.25GHz operation
DJ=33.1ps=0.041UI



1.06GHz operation
DJ=29.4ps=0.031UI

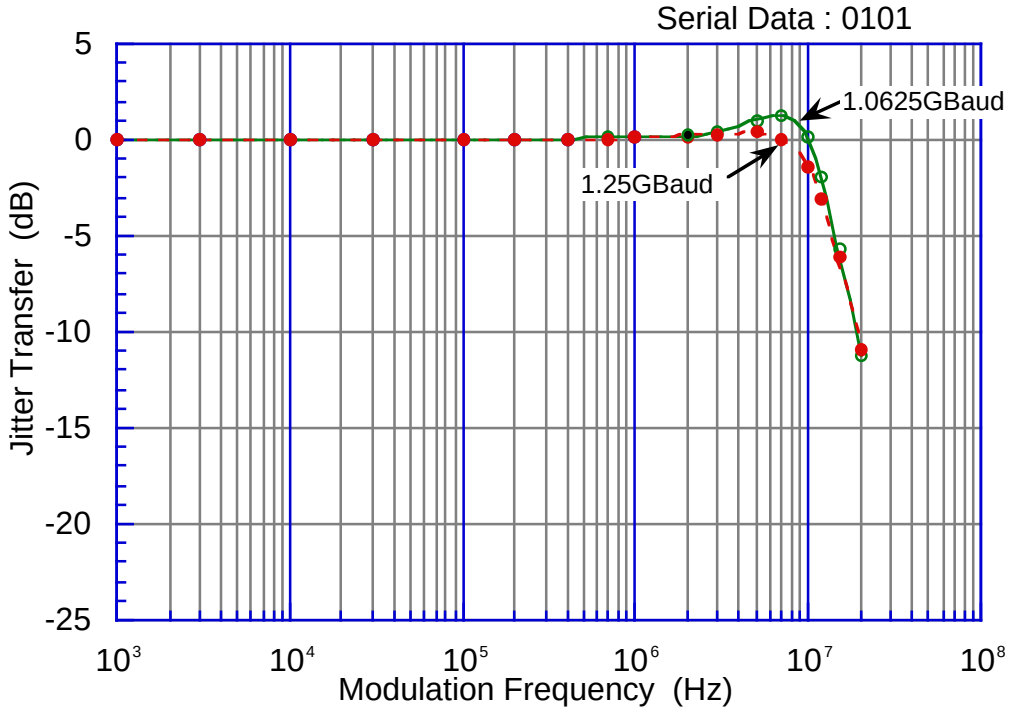




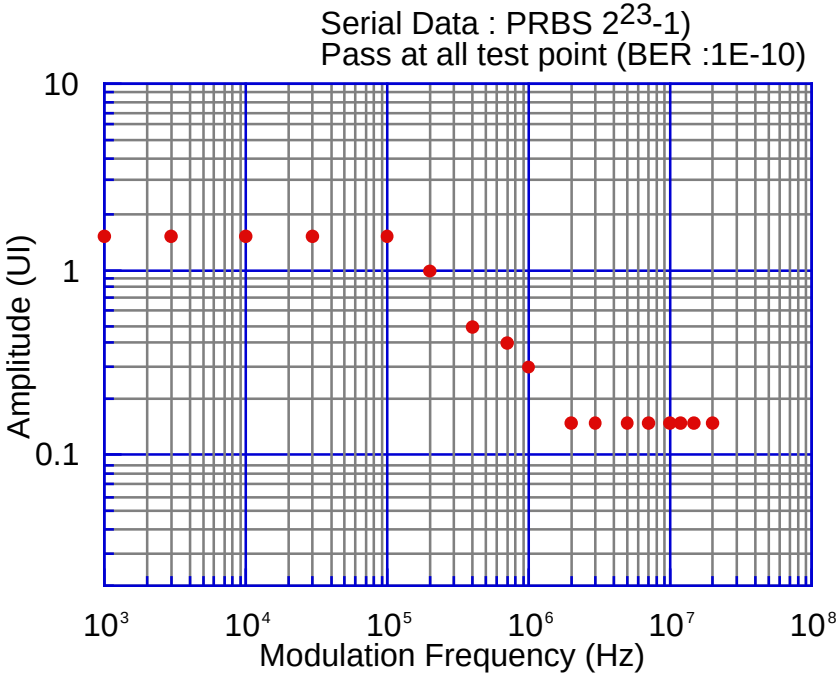
CXB1584Q RX Characteristics on Single REFCLK operation

Jitter Transfer & Jitter Tolerance

Jitter Transfer



Jitter Tolerance



Conventional Single REFCLK Operation

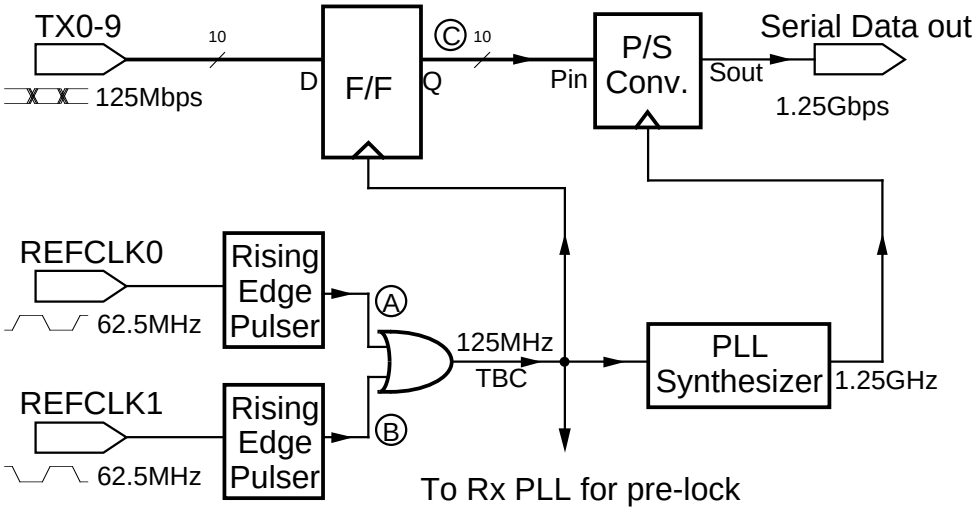
Characteristic comparison between 1.25Gbaud and 1.06Gbaud

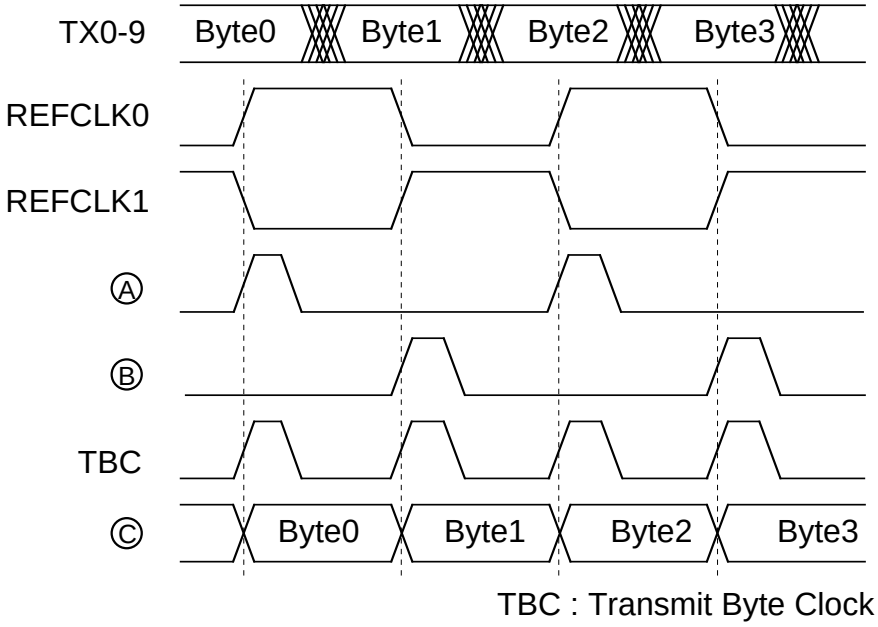
		1.25Gbaud operation	1.06Gbaud operation
TX	RJ (14σ)	0.135 UI (7.7 ps RMS)	0.137 UI (9.2 ps RMS)
	DJ (Peak to Peak)	0.036 UI	0.042 UI
	Total Jitter (RJ+ DJ)	0.171 UI	0.179 UI
	PLL Band Width (-3dB)	13.7 MHz	15.2MHz
RX	RJ on FC Idle pattern (14σ)	0.123 UI (7.0 ps RMS)	0.128 UI (8.6 ps RMS)
	DJ (Peak to Peak)	0.041 UI	0.031 UI
	Total Jitter (RJ+ DJ)	0.161 UI	0.159 UI
	PLL Band Width on 0101 pattern (-3dB)	11.9 MHz	12.3 MHz

Half rate Dual Reference Clock Operation

Advantages over Single Reference Clock Operation

- **Output speed requirement for pre-stage(CMOS) of transmitter becomes half (62.5MHz)**
- **Noise caused by REFCLK0 & REFCLK1 is canceled.**



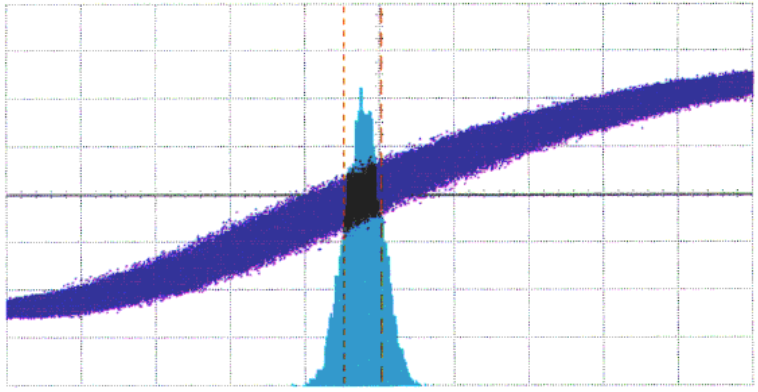


TBC : Transmit Byte Clock

CXB1584Q TX Characteristics on Half Rate Dual REFCLK operation

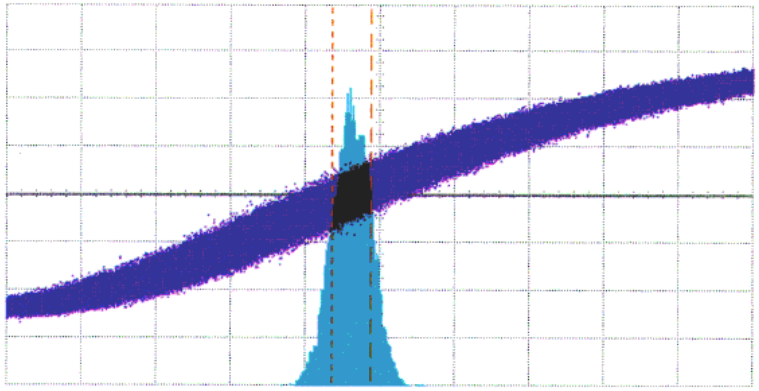
Random Jitter

Transmit Bit Clock on Dual REFCLK
Bit Rate=1.25Gbaud
RJ(14σ)=105.0ps=0.131UI



Time base : 30 ps/div
Vertical axis : 100 mV/div
σ=7.5 ps

Transmit Bit Clock on Single REFCLK
Bit Rate=1.25Gbaud
RJ(14σ)=107.8ps=0.135UI

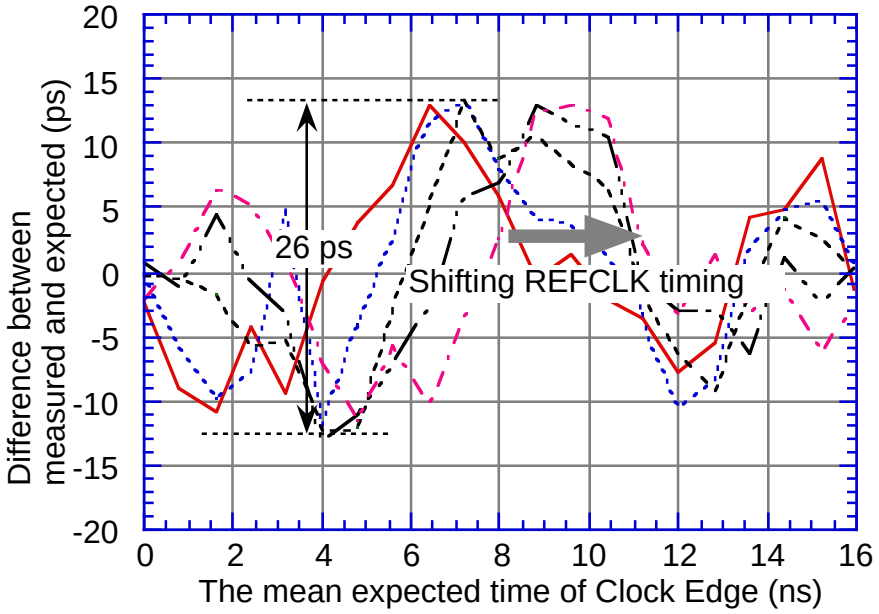


Time base : 30 ps/div
Vertical axis : 100 mV/div
σ=7.7 ps

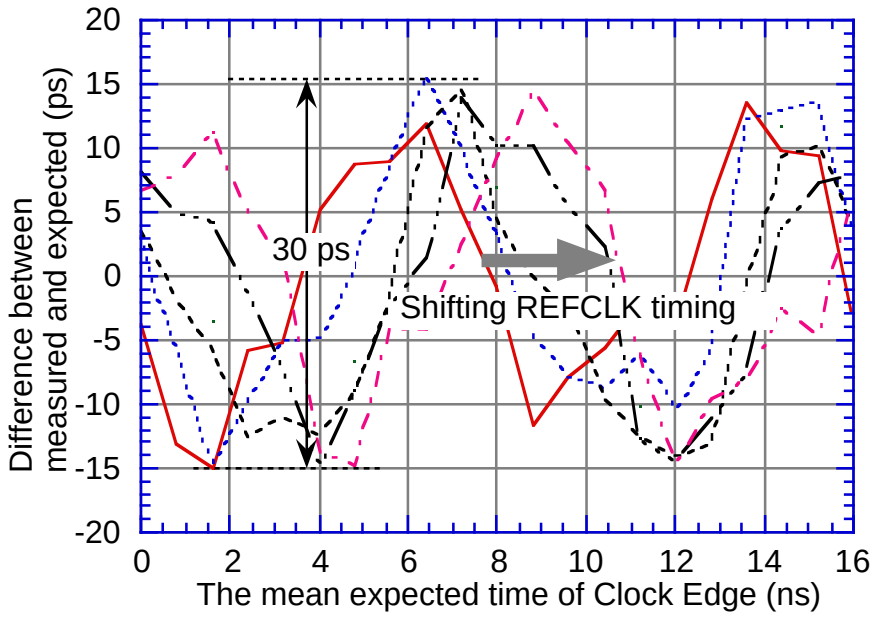
CXB1584Q TX Characteristics on Half Rate Dual REFCLK operation

DJ Measurement of Transmit bit clock

Half Rate Dual REFCLK (62.5MHz)



Single REFCLK (125MHz)

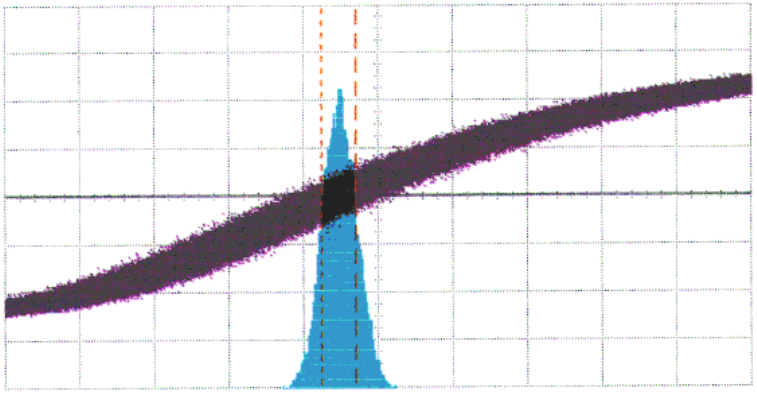


CXB1584Q RX Characteristics on Half Rate Dual REFCLK operation

Random Jitter

Recovery clock on Dual REFCLK
Bit Rate = 1.25GBaud
RJ(14σ)=96.6ps=0.121UI

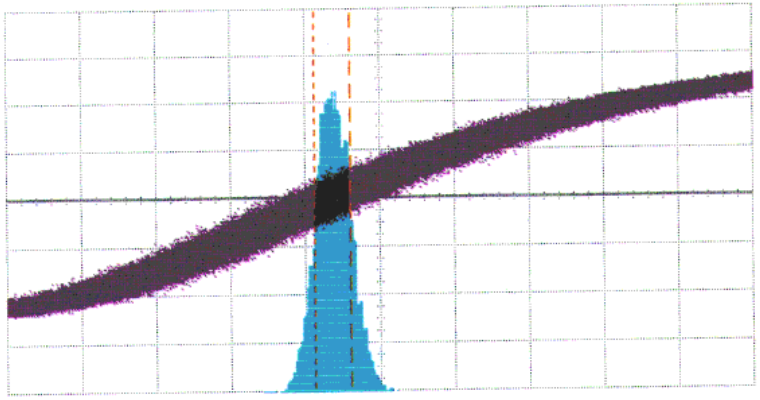
Serial Data : FC Idle (T.D.=80%)



Time base : 30 ps/div
Vertical axis : 100 mV/div
σ=6.9 ps

Recovery clock on Single REFCLK
Bit Rate = 1.25GBaud
RJ(14σ)=98.0ps=0.123UI

Serial Data : FC Idle (T.D.=80%)



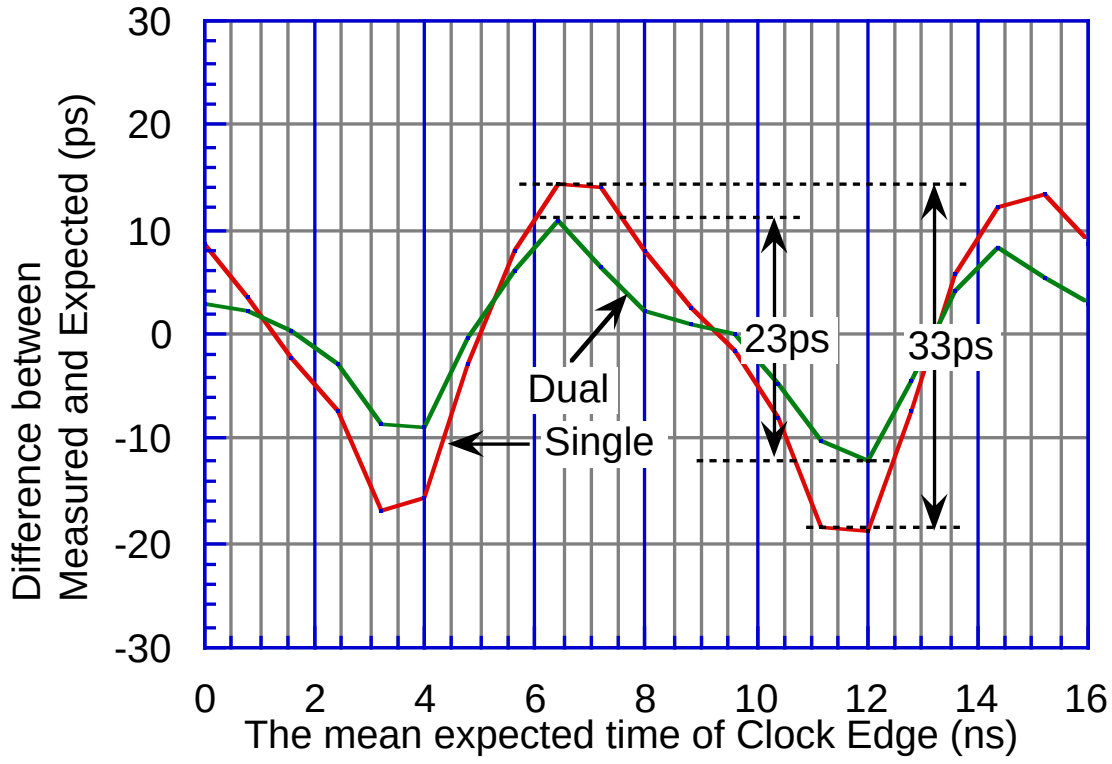
Time base : 30 ps/div
Vertical axis : 100 mV/div
σ=7.0 ps

CXB1584Q RX Characteristics on Half Rate Dual REFCLK operation

DJ Measurement of Recovery clock

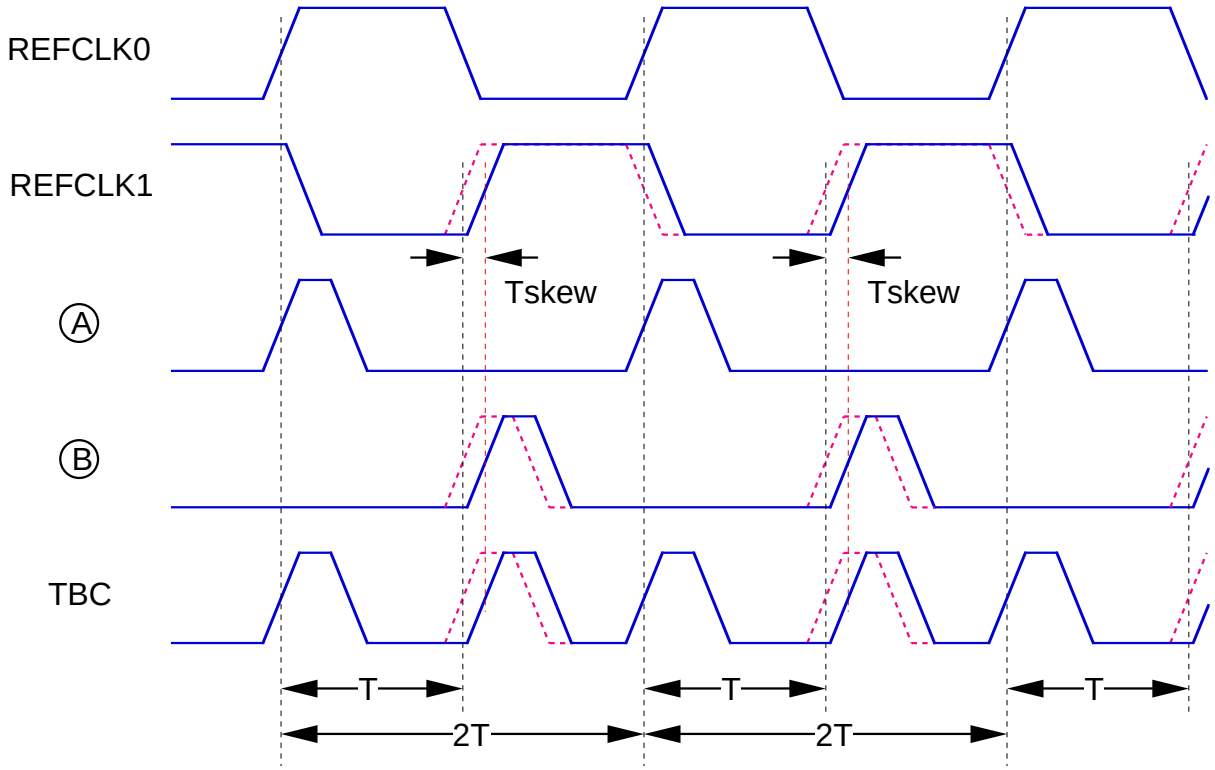
(Serial Data : ±K28.5)

Dual REFCLK (62.5MHz) : DJ=23ps=0.029UI
Single REFCLK (125MHz) : DJ=33ps=0.041UI



TBC Jitter induced by REFCLK skew

TBC is phase-modulated at 62.5MHz(1/2T)

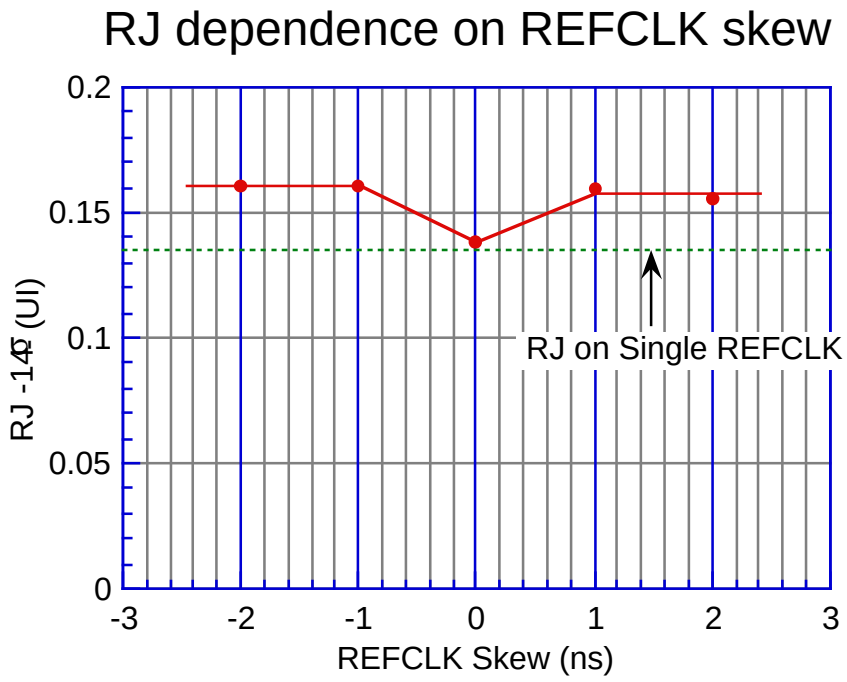


T = 1/125MHz = 8ns

REFCLK skew Influence on TX Jitter

Random Jitter

RJ of Tx with skewed REFCLK is larger than one with non skewed REFCLK.
But it becomes constant over 1ns skew.

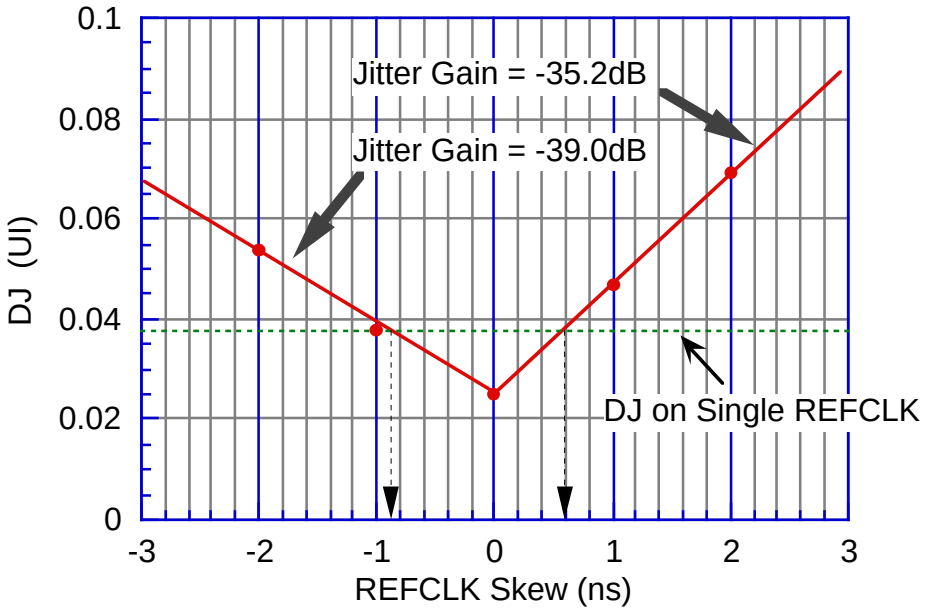


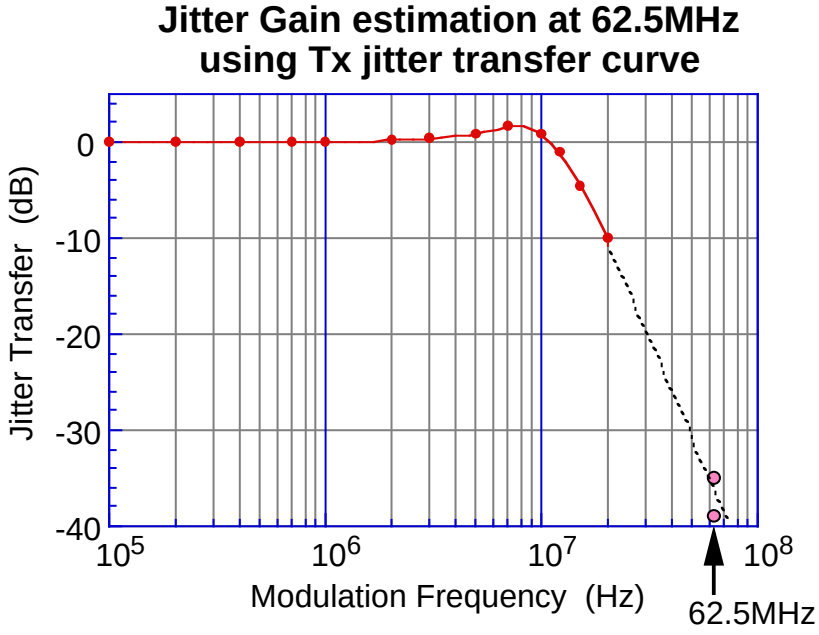
REFCLK skew Influence on TX Jitter

Deterministic Jitter

TX_PLL transfers TBC jitter to Serial Data output.
But its gain is very small.
This depends on the jitter transfer characteristics.

DJ dependence on REFCLK skew



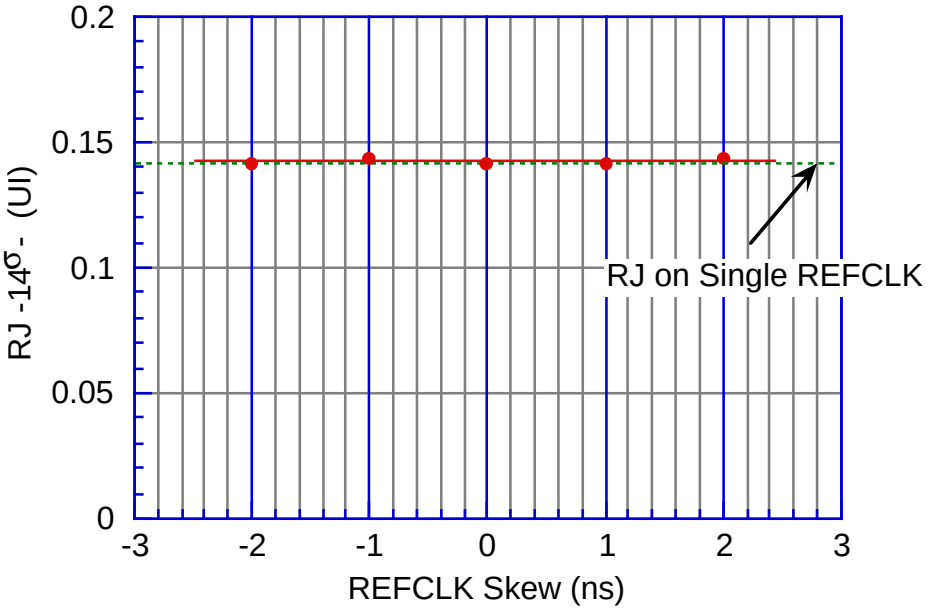


REFCLK skew Influence on RX Jitter

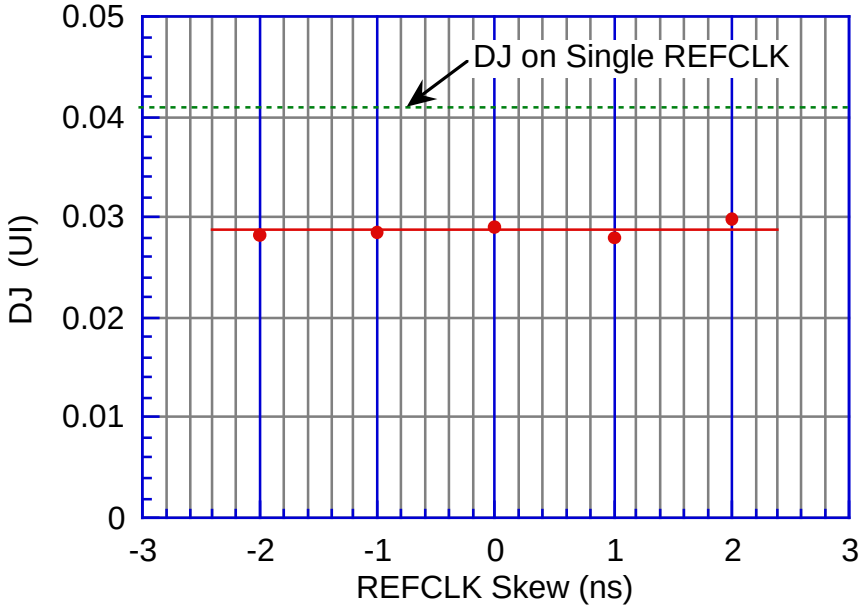
RJ & DJ of Recovery Clock (Serial Data : ±K28.5)

DJ on Dual REFCLK is smaller than on Single REFCLK.
This result shows that noise caused by Reference Clock is reduced in comparison to Single REFCLK.

RJ dependence on REFCLK skew



DJ dependence on REFCLK skew



CXB1584Q Characteristics at 1.25Gbaud

Dual REFCLK operation comparison with Single REFCLK

		Dual REFCLK (Skew = 0ns)		Dual REFCLK (Skew = ±2ns)	Single REFCLK
TX	RJ (14σ)	0.131 UI (7.5 ps RMS)	Δ	0.161 UI (9.2 ps RMS)	0.135 UI (7.7 ps RMS)
	DJ (Peak to Peak)	O 0.033 UI	Δ	0.069 UI	0.038 UI
	Total Jitter (RJ + DJ)	O 0.164 UI	Δ	0.230 UI	0.173 UI
RX	RJ on ±K28.5 (14σ)	0.142 UI (8.1 ps RMS)		0.144 UI (8.2 ps RMS)	0.142 UI (8.1 ps RMS)
	DJ (Peak to Peak)	O 0.029 UI	O	0.030 UI	0.041 UI
	Total Jitter (RJ + DJ)	O 0.171 UI	O	0.174 UI	0.183 UI

O : Better than Single REFCLK.
Δ : Worse than Single REFCLK.
The others are almost same as Single REFCLK.

Conclusion

1. CXB1584Q has shown excellent performance at 1.25Gbaud in the conventional single REFCLK operation.
   (Total Jitter Tx : 0.173 UI, Rx : 0.183 UI)

2. In the half rate dual REFCLK operation SONY propose, CXB1584Q has shown slightly better performance at 1.25Gbaud compared with the conventional operation.
   (Total Jitter Tx : 0.164 UI, Rx : 0.171 UI)

3. In the skewed dual REFCLK operation, the jitter characteristics of Tx has been degraded a little bit, however those are still good enough for practical datacom application.
   (Total Jitter Tx : 0.230 UI, Rx : 0.174 UI)

4. Using the half rate dual REFCLK operation, output speed requirement at REFCLK driver has been reduced to 62.5MHz, and noise caused by REFCLK has been reduced significantly.