Timing Analysis of Option C Clocking Scheme for Gigabit Ethernet SERDES and MAC devices

Haluk Aytac
High Speed I/O Products
Hewlett-Packard Company
350 West Trimble Road
San Jose, CA 95131

408 435 4246 haluk_aytac@hp.com

INTRODUCTION:

This note analyzes the timing requirements for Option C (Figure.1). There are relationships among timing parameters for PHY, MAC IC's and also board layout.

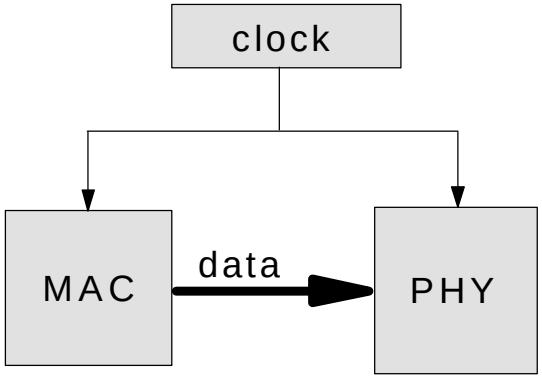

Figure. 1 Option C Clocking Scheme

TIMING PARAMETERS:

Table I shows the important parameters and the entity each is associated with.

Name	Association	Figure	Definition
Td	MAC	2	delay from C_{MAC} to data out of MAC
Tdd	PCB	4,5	delay from data out of MAC to data into PHY
Ts	PHY	3	setup time for data into PHY
Th	PHY	3	hold time for data into PHY
C_{MAC}	PCB	4,5	clock delay from clock source to clock into MAC
C_{PHY}	PCB	4,5	clock delay from clock source to clock into PHY

Table I

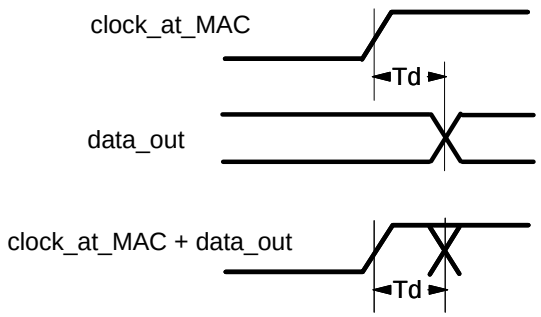

Figure. 2 MAC parameter

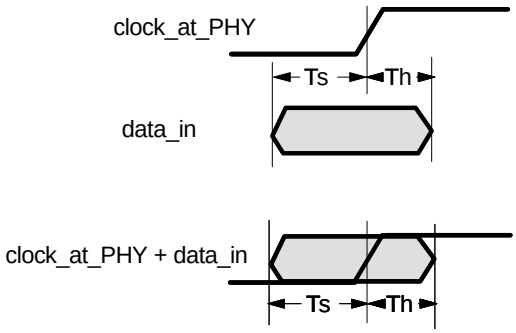

Figure. 3 PHY parameters

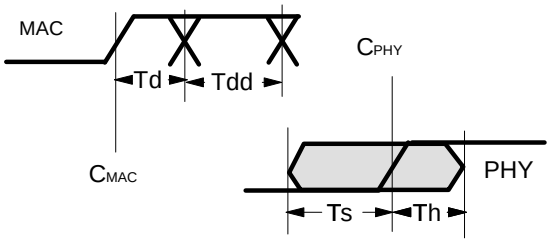

Figure. 4 MAC, PHY, case A

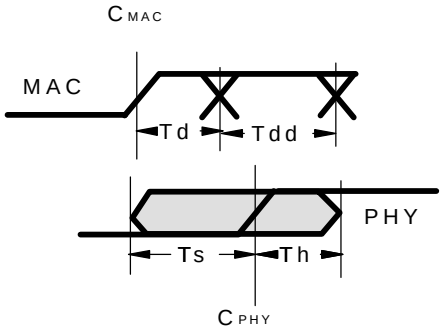

Figure. 5 MAC, PHY, case B

ANALYSIS:

For reliable operation,

RULE: data should not change within the Ts + Th window at the PHY device. This may be achieved in two ways:

A. PHY gets data from the current clock on MAC (Figure. 4)

B. PHY gets data from the previous clock on MAC (Figure. 5)

To satisfy the rule, we have to satisfy the following equations for each case:

A. $C_{PHY} - C_{MAC} >= Td + Tdd + Ts$

B. $C_{MAC} - C_{PHY} >= Th - Td - Tdd$

Case A is not attractive as it gets current data. It is also harder to achieve as a difference in clock delays (which should be small) has to be greater than a sum of 3 delays.

We concentrate on case B.

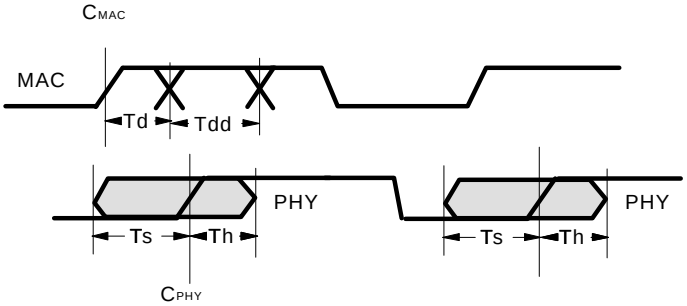

Figure. 6 Case B setup condition

With the following definitions:

$D = C_{MAC} - C_{PHY}$

$Td' = Td + Tdd$

and adding the setup equation (Figure. 6), we have the two equations for Case B in one place:

$D >= Th - Td'$

$T_{CY} >= D + Td' + Ts$, where T_{CY} is the cycle time (8ns) (Figure. 6)

which can also be written as:

$Th =< Td' + D =< T_{CY} - Ts$

The maximum values of Td', D obey the following equation:

$Td'_{MAX} + D_{MAX} = T_{CY} - Ts$

The minimum values of Td', D obey the following equation:

$Td'_{MIN} + D_{MIN} = Th$

Now, require that:

$D_{MAX} + D_{MIN} = 0$

This is fair to ask as this is the delay difference of clocks. One or the other clock may be ahead of the other. This condition yields:

$(D_{MAX} - D_{MIN}) / 2 + (Td'_{MAX} - Td'_{MIN}) / 2 = (T_{CY} - Ts - Th) / 2$

$(Td'_{MAX} + Td'_{MIN}) / 2 = (T_{CY} - Ts + Th) / 2$

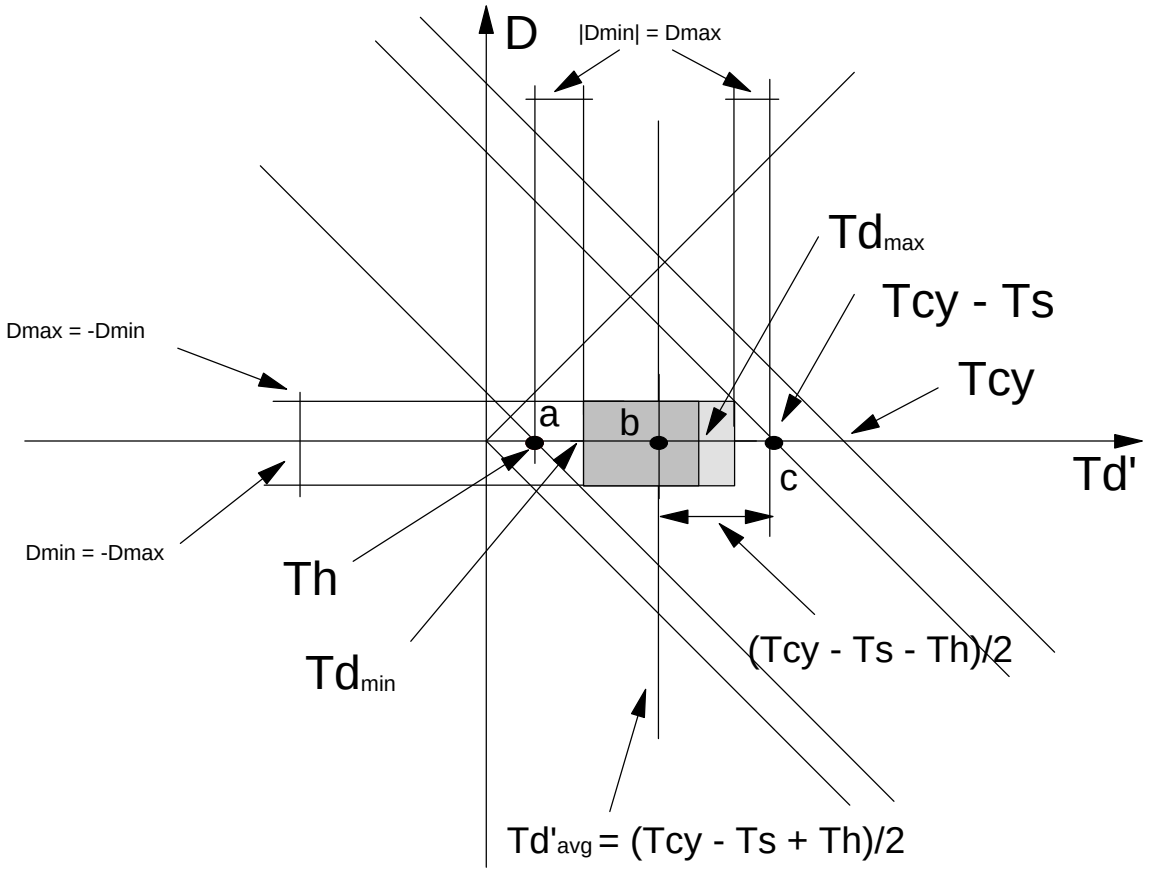

Figure. 7

Working with Figure. 7, we can determine Td' given Ts, Th and $D_{MAX} = -D_{MIN}$. The abscissa is Td' and the ordinate is D.
01. Mark the cycle time Tcy (8ns) on the abscissa.
02. Subtract Ts and mark point (c).
03. Mark Th from origin as point (a). Td' at best can range from (a) to (c) if $D_{MAX} = -D_{MIN} = 0$.
04. Mark the midrange i.e. Td'avg at point (b). Its abscissa value is (Tcy - Ts + Th) / 2.
05. Decide what your uncertainty in difference of clock delays to MAC and PHY will be (D_{MAX}) .
06. Move left from (c) with this value. You just identified Td'_{MAX}.
07. Find the symmetrical point around (b) on the abscissa. This is Td'_{MIN}.

Note that Td' = Td + Tdd.

$Td_{MIN} = Td'_{MIN} - Tdd_{MIN}$ (assume 0 for safety)
$Td_{MAX} = Td'_{MAX} - Tdd_{MAX}$

The range for Td and D are then defined by the darker shaded box in Figure. 7.

Practical examples:

Ts = 2
Th = 1
$D_{MAX} = 0.5$
$Tdd_{MAX} = 1$

yields a Td range of 1.5-4.5 ns.

Ts = 1.5
Th = 1.5
$D_{MAX} = 0.5$
$Tdd_{MAX} = 1$

yields a Td range of 2.0-5.0 ns.

COMPONENTS OF Tcy:

The following are the components of one Gigabit Ethernet clock cycle (clock at PHY device).
Tcy (standard) = Th (PHY) + D range (PCB) + Td range (MAC) + Tdd range (PCB) + Ts (PHY)