

# **Gigabit PCS for PAM 3x3**

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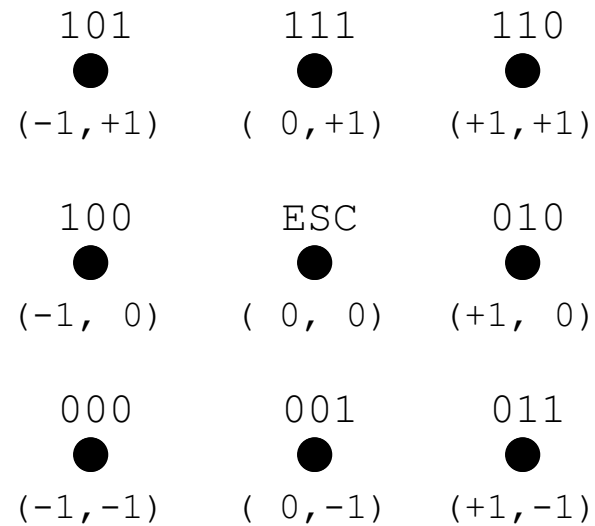
## Objectives

- **Support the CSMA/CD MAC**
- **Support GMII, Repeaters, Auto-Negotiation**
- **Provide 1000Mb/s data rate at GMII**
- **Full Duplex Operation**
- **Simple Implementation**



# Digital Mapping to PAM 3 x 3

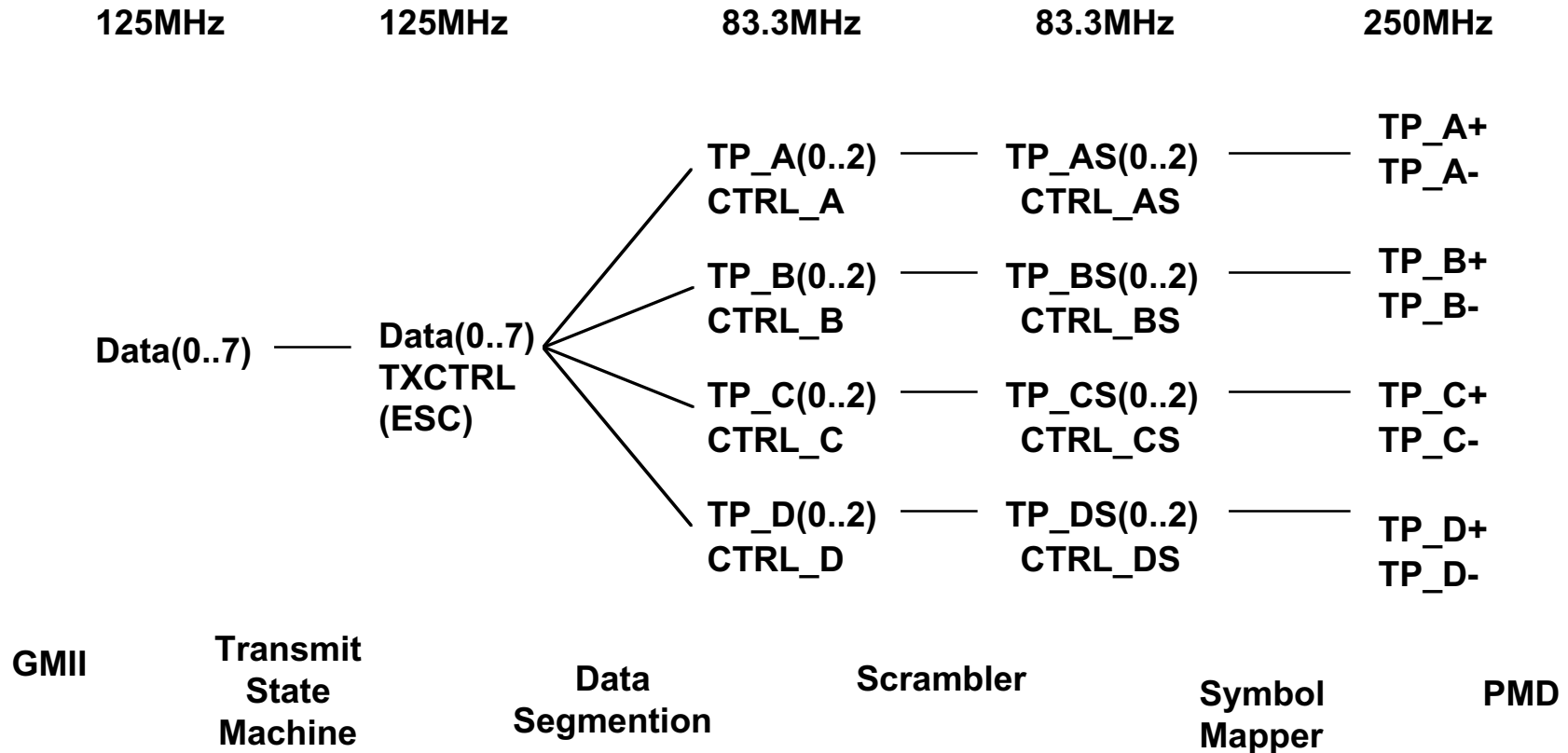
Data	I	Q
(000)	(-1, -1)	
(001)	( 0, -1)	
(011)	(-1, 0)	
(010)	(-1, 1)	
(110)	(+1, 0)	
(111)	(+1, -1)	
(101)	(+1, +1)	
(100)	( 0, +1)	
(ESC)	( 0, 0)	



(Before Scrambling)



# Digital Perspective of Transmit Data Path



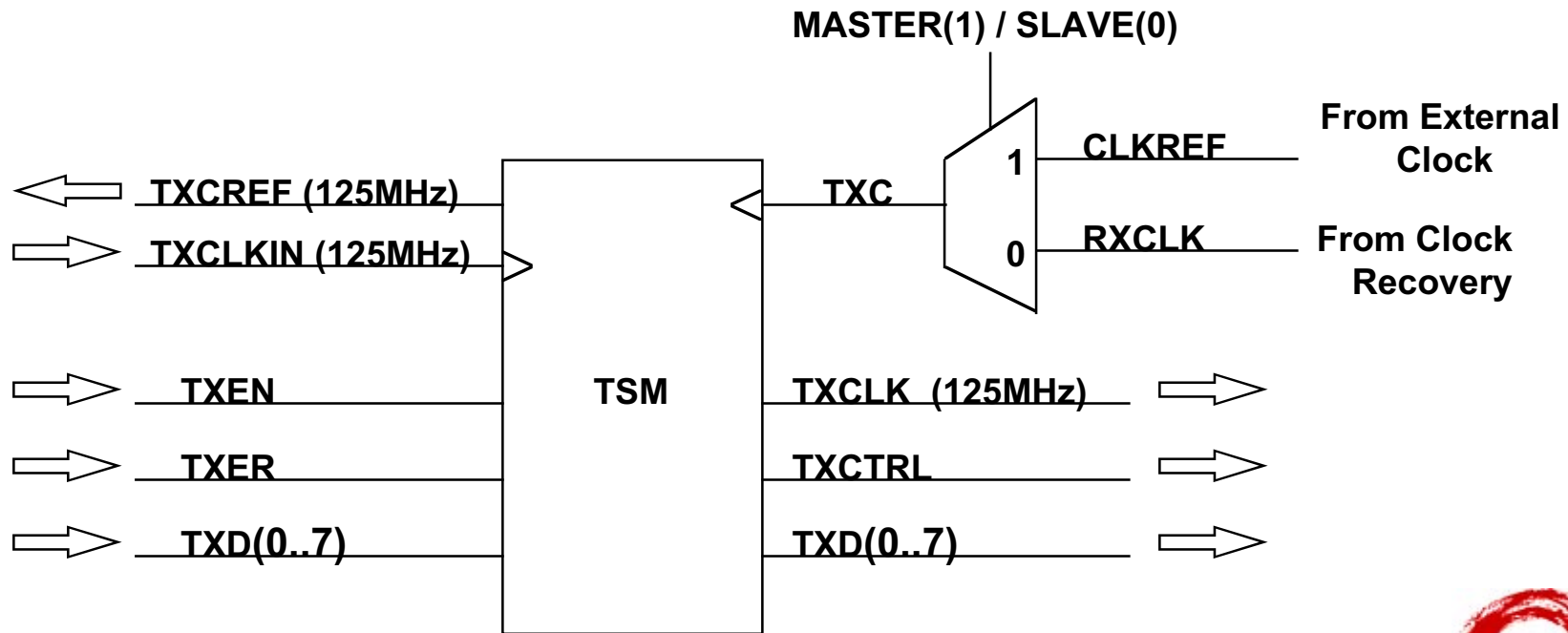
## GMII

- **Transmit Interface**
  - TXCLK provided from PHY (referenced to TXCLKIN)
  - 8 Bit Data Path
  - Carrier Extension Support
- **Receive Interface**
  - RXCLK provided from PHY
  - 8 Bit Data Path
  - Carrier Extension Support
- **TSC Interface (optional)**
  - Support for 32 control codes



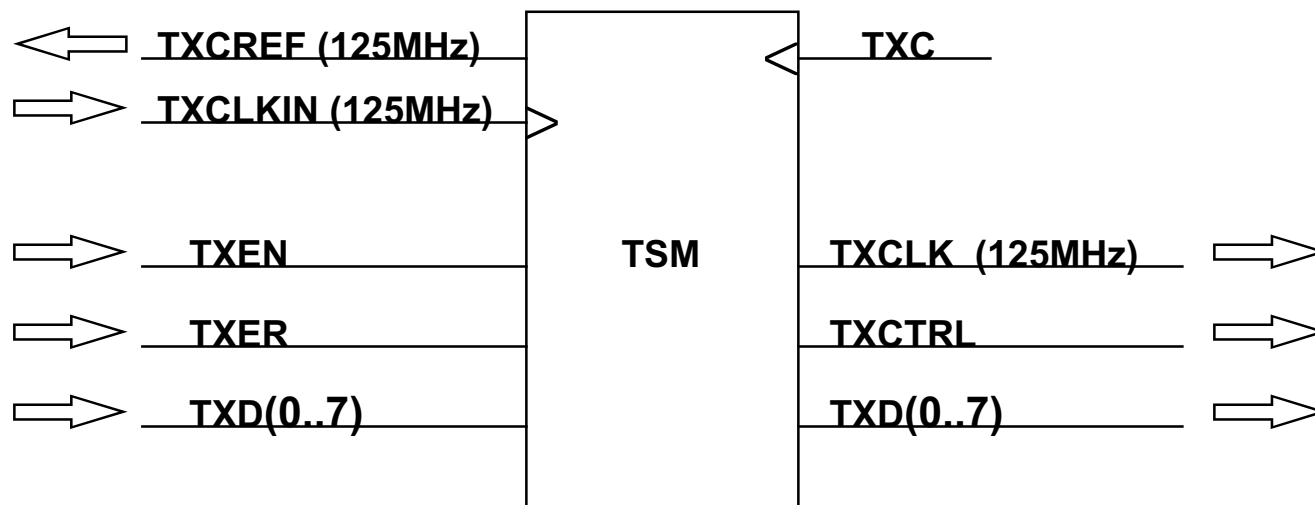
# Transmit GMII Interface - Clock

- Clock Reference source is dependent on PHY location
  - Master when PHY is in a HUB
  - Slave when PHY is in a station
- ECHO cancellation requires synchronized timing



## Transmit State Machine Function

- Encapsulation of Frame from MAC
  - (SOF/EOF/CRSEXT)
- Error Code Generation
- Idle Generation
  - Idle Code
  - Twisted Pair I.D. Code



# Idle Code Function

- **Data sent on all 4 pairs**
- **Different pairs have up to 40ns skew**
- **Scheme needed to determine the skew between the different pairs**
  - **Allows for polarity correction**
  - **Allows for pair swapping**





# Idle Code Scheme

- Send the general IDLE byte all pair (11111111)
- Every 3 x n bytes simultaneously send the unique TP ID CODE for each individual pair
- Receive side measures skew of each pair for proper data deskewing

Sent Out Of PHY

I	I	I	I	I	TP1	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	
I	I	I	I	I	TP2	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I
I	I	I	I	I	TP3	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I
I	I	I	I	I	TP4	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I

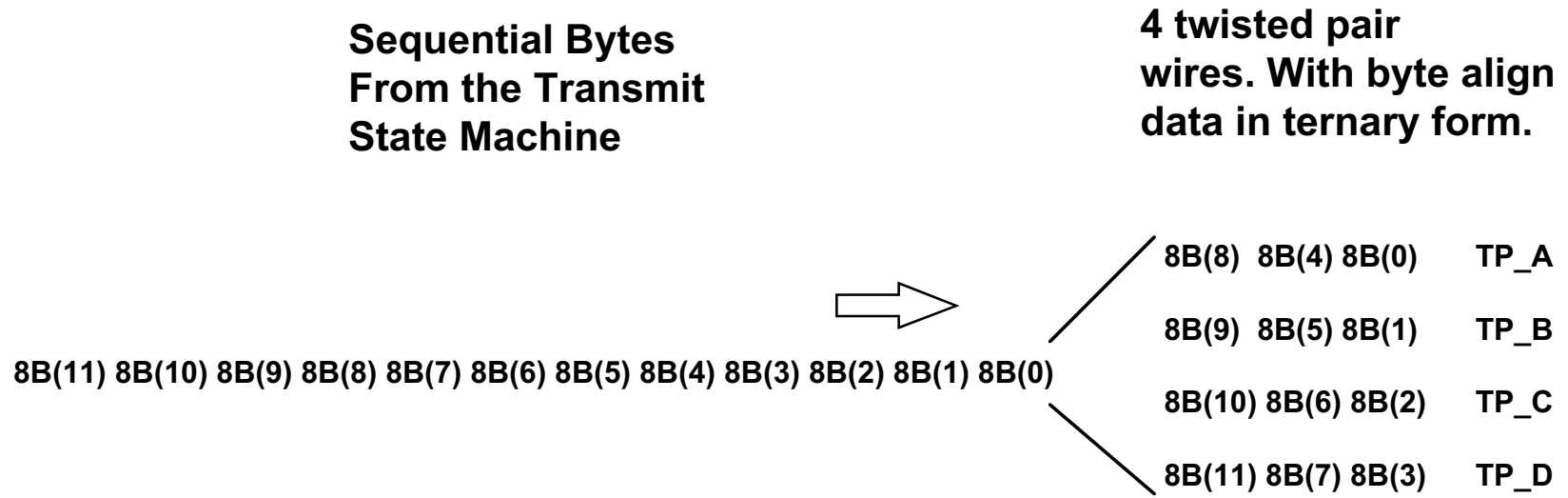
Received by Remote PHY

I	I	I	I	I	TP1	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	
I	I	I	I	I	I	I	TP2	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I
I	I	I	I	I	I	I	TP3	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I
I	I	I	I	I	I	I	I	TP4	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I



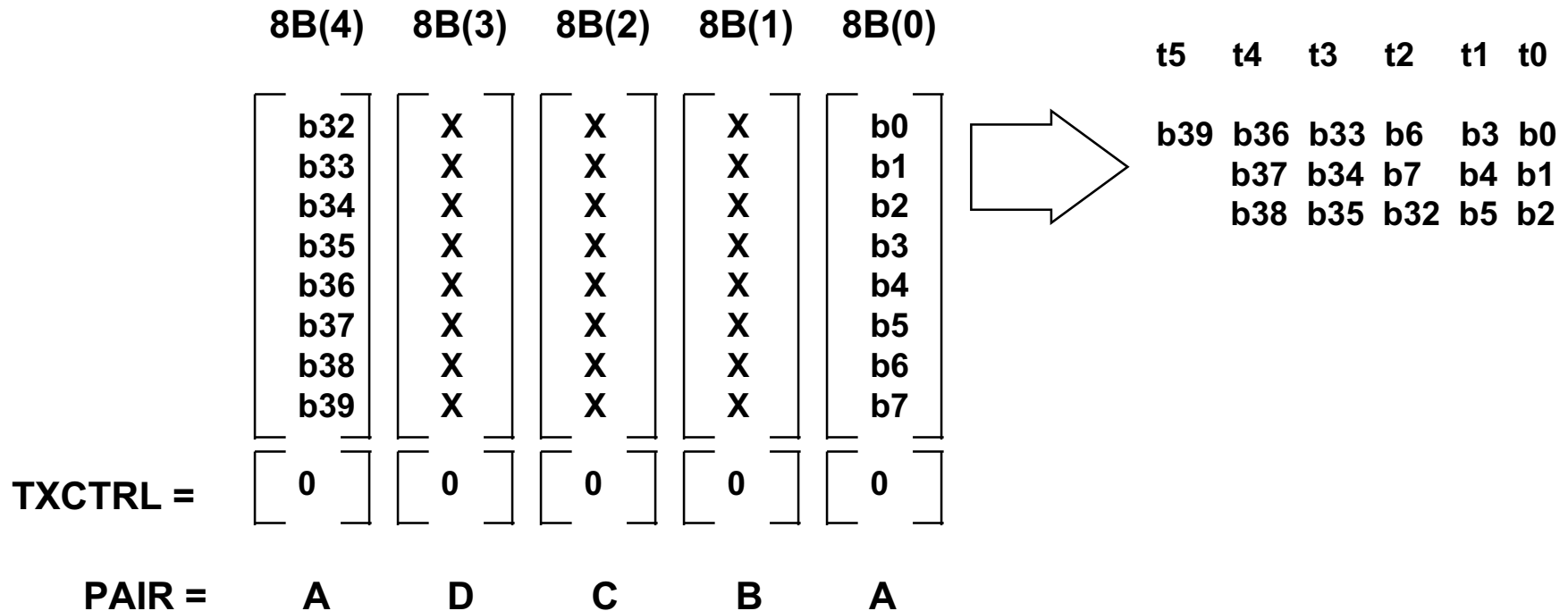
# Data On The Wire

- A byte is divided into ternary values and then sent down a twisted pair.
- The next byte is sent onto the next twisted pair.



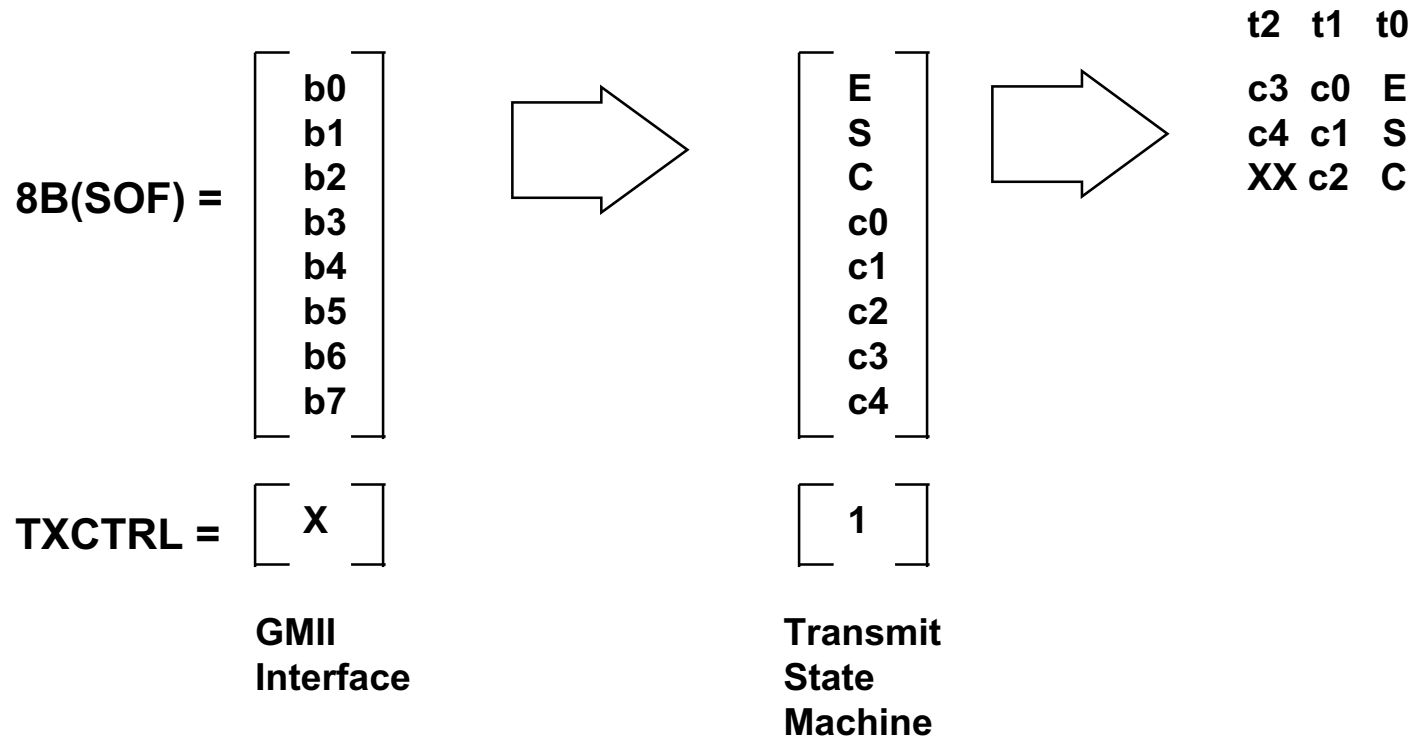
# 8 Bit Data Conversion To Ternary

- Each Byte is time multiplexed to 2.6 ternary values



# Control Signal Sequence

- The first three bits are the ESC symbol followed by 5 control bits.



# Definition: Control Bits

- Bit selection minimizes error possibility

	C0	C1	C2	C3	C4
SOF	1	0	0	0	0
EOF	0	1	0	1	0
CRSE	0	0	1	1	1
HALT	0	1	1	0	0
TP1	1	0	1	0	0
TP2	1	1	0	0	1
TP3	1	0	0	1	1
TP4	1	0	1	1	0

t2 t1 t0  
c3 c0 E  
c4 c1 S  
XX c2 C



# Scrambler

- Helps clock recovery
- Flattens the spectrum (EMC)
- Individual Scramblers per pair simplifies data descrambling
- Ternary scrambler
- Possible Generator polynomials:

$$G(D) := 1 + 2D + D^{13}$$

$$G(D) := 1 + 2D^4 + D^{13}$$

$$G(D) := 1 + 2D^6 + D^{13}$$

$$G(D) := 1 + 2D^7 + D^{13}$$

$$G(D) := 1 + 2D^9 + D^{13}$$



## Bit Budget

- **Transmit**
  - TXEN to MDI = 12 Byte Times
- **Recieve**
  - MDI to CRS,COL Assertion = 14 Byte Times
  - MDI to RXDV Assertion = 18 Byte Times



## Work To Be Done

- **Selection Of Scrambler Polynomial**
- **Definition Of Control Codes**
- **Define Receive Path**

