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Title: Physical Layer Proposal for 1 Gbit/s Full / Half Duplex Ethernet Transmission over Single (4-pair) or Dual (8-pair) UTP-5 Cable.

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Abstract
The extension of the current IEE802.3 specifications to support a bit rate of 1Gbps is currently under investigation by the HSSG. These bit rates are regarded to be essential to support the high bandwidth requirements of mixed 10BASE and 100BASE networks, and many applications requiring a dedicated high speed link to a server.
The HSSG has already made excellent progress in the way of defining 1000BASE for fibre. This contribution outlines an approach for supporting 1Gbps, either half or full-duplex, over single (4-pair) or dual (8-pair) unshielded twisted pair category 5 (UTP-5) cable.

Notice
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Physical Layer Proposal for 1 Gbit/s Full / Half Duplex Ethernet Transmission over Single (4-pair) or Dual (8-pair) UTP-5 Cable

Version 1.0

September 1996

1. Introduction

This contribution describes the Physical Layer components required to support transmission of Ethernet frames at 1Gbps full duplex data rate carried over single or dual UTP-5 cable. Transmission over a standard 4 pair UTP-5 bundled cable would provide a reach of 50m, and transmission over 2 such standard bundled cables would provide a reach of 100m. The method is suitable for both full and half duplex modes of operation.

Operation with single and dual cables is shown in Fig 1. below:

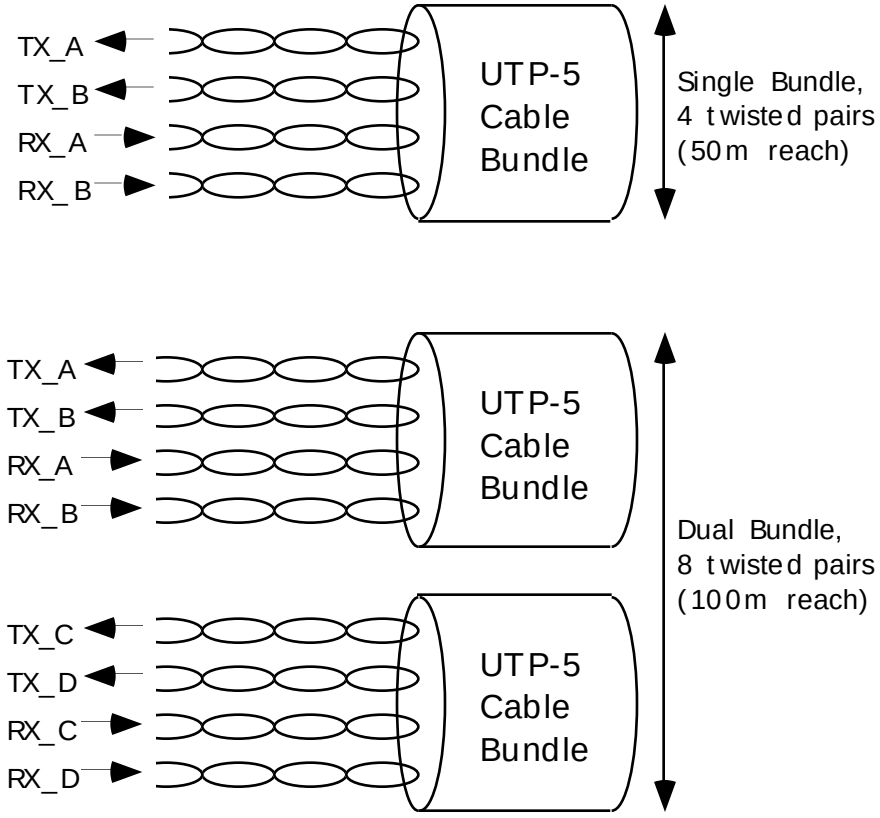


Fig 1. Operation with Standard Single or Dual UTP-5 Cable Bundles

In full duplex mode, a single cable would use 2 pairs for transmit and 2 pairs for receive, each pair carrying 500Mbps of data. Alternatively, dual cables could be used to double the reach to 100m, 4 pairs being used for transmit and 4 pairs for receive, each pair carrying 250Mbps. With full duplex there is no need for higher layers to support the CSMA/CD protocol as the connection would be point to point.

In half-duplex mode, a similar transmit and receive scenario would exist with either single or dual cables, but the higher layer would need to implement the CSMA/CD protocol.

There are numerous problems in trying to transmit data at these rates using only unshielded twisted pairs (UTP-5) as the medium. These may be summarized as follows:

- Signal degradation due to cross-talk (near end and pair-pair).
- Signal attenuation due to lossy medium.
- Limitation of launch power due to FCC compliance.

This paper discusses a method to overcome these problems. The method chosen aims to provide the means to allow a possible low cost but robust implementation using today's available technology, and not requiring advanced computationally expensive DSP implementations.

The method uses a 2 bit to 4 level coding scheme in order to reduce the effective symbol rate on each pair of UTP-5 cable. By using 4 level encoding, the symbol rate on each pair is reduced to either 250MBaud or 125MBaud, depending on the number of pairs. By limiting the transmit launch power of these symbols, and by specifying a maximum cable distance of either 50m or 100m, the power density spectrum can be controlled to meet FCC-B emission standards, while still providing sufficient signal at the receiver to enable reception with a BER of better than 10^{-10}.

This paper first discusses an overview of the technique, followed by a mathematical analysis and associated simulation results, and concludes with empirical results derived from lab experiments using a discrete implementation of the method.

2. 1000BASE-CX Functional Overview

The components required to implement a 1Gbps PHY may be divided into the following sub layers within the PHY layer:

- Gigabit Media Independent Interface (GMII)
- Physical Coding Sublayer (PCS)
- Physical Media Attachment (PMA)
- Physical Media Dependent (PMD)

These components may be mapped into an identical protocol stack as illustrated in IEEE802.3u (100BASE-X), with the modification of the GMII and naturally the MDI. This is illustrated in Fig. 2 below:

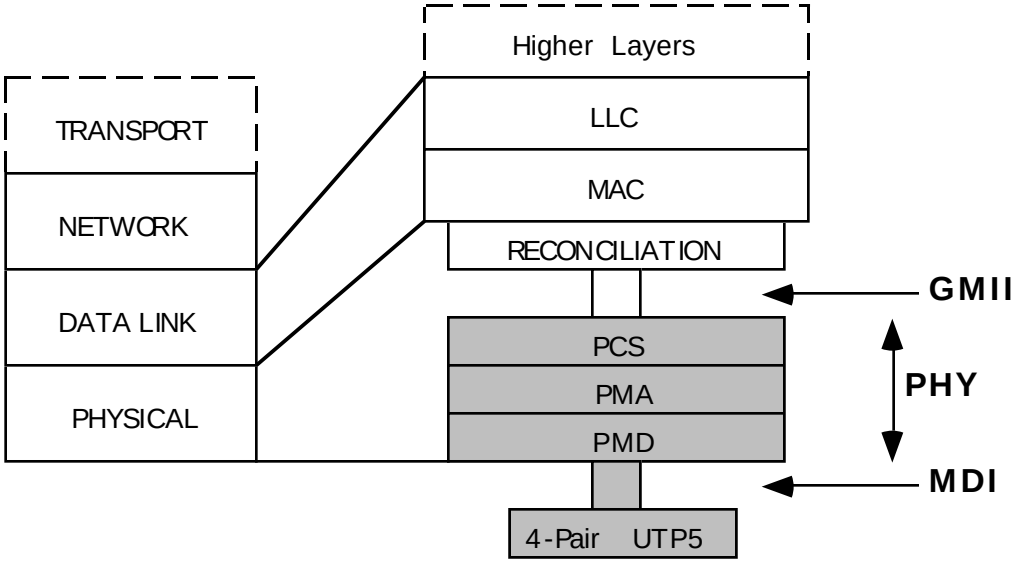


Fig. 2 Architectural Positioning of 1000BASE-CX

The architectural positioning of 1000BASE-CX shown in Fig. 2 maps to the normal view of the protocol stack as described in IEEE802.3 documents. To clarify the proposed solution, the following provides a brief overview without separating the different functions into the appropriate sub-layers.

A simplified block diagram of the 4-pair solution is illustrated in Fig. 3. The 8-pair solution is similar, but uses 4 processing paths for both transmit and receive.

For the sake of brevity, the remainder of this proposal refers to the single cable (4-pair) case, unless otherwise noted.

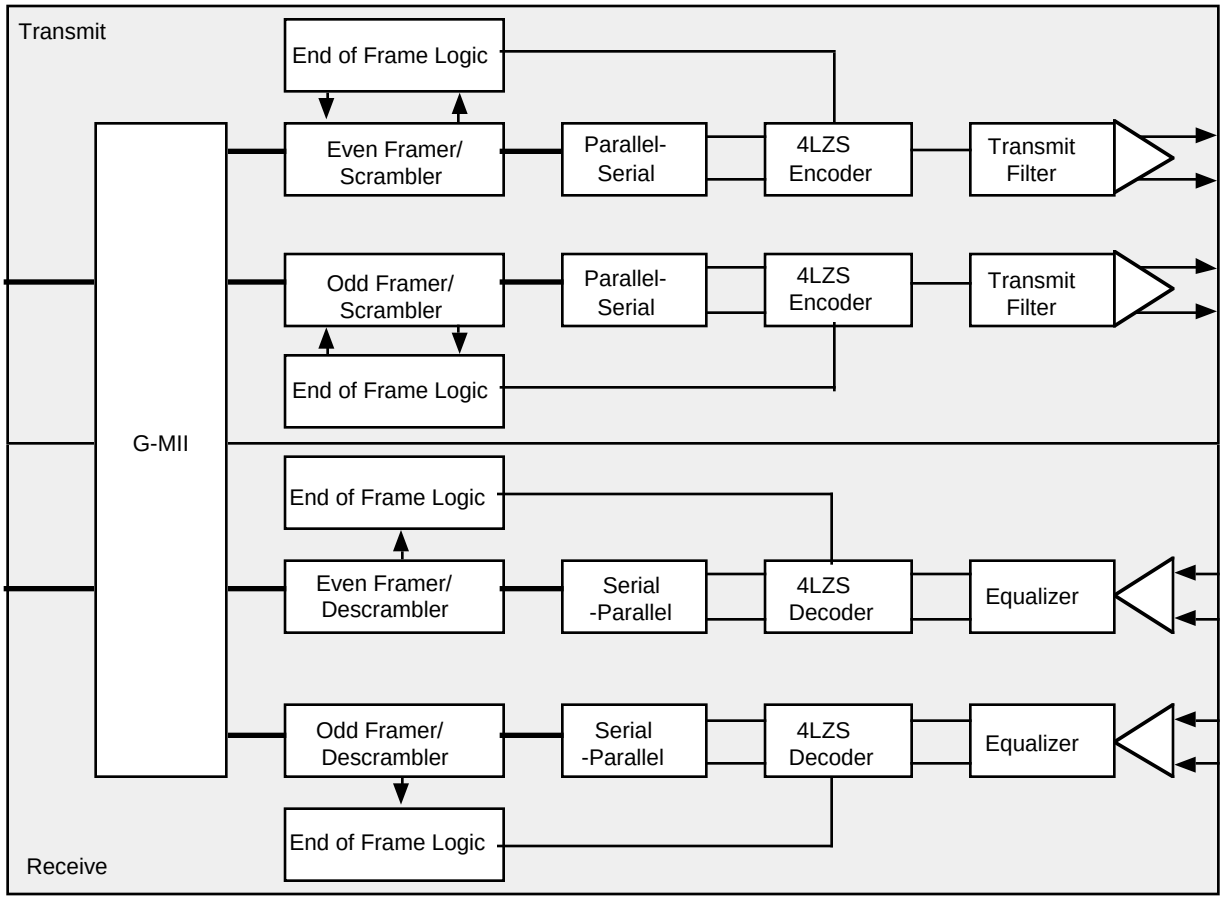


Fig. 3 Block Diagram of 1000BASE-CX

In the transmit path:

- Accept byte aligned date over the GMII at 125Mbytes/s.
- Demultiplex into two parallel byte streams at 62.5Mbytes/s.
- For each parallel stream, map the split ethernet frame into a physical layer stream.
- Scramble the entire frame excluding the preamble bytes using a self synchronous scrambler to provide spectral shaping.
- Map the resulting serial bit stream into quats (using 4LZS signal coding).
- Transmit the 4 level signals (from the 2 parallel streams) to the 2 transmit pairs of UTP-5.
- At the end of the frame, transmit a null code for 4 symbol periods, then a control byte followed by idle codes.

In the receive path:

- Receive the 4 level signals from the 2 transmit pairs of UTP-5.
- Map the resulting quats into a serial bit stream (using 4LZS signal coding).
- Search for the start of packet by verifying a transition from the idle code to the preamble code.
- Having received frame and byte alignment, synchronize with the other stream framing block.
- Pass each byte stream to a multiplexer for frame re-generation (one stream known to contain the first byte), and pass to the GMII for transmission.
- For each stream, search for the end of the packet by detecting a null transmission on the line existing for 4 symbol periods, followed by a control code.
- Having correctly detected the end of packet for each stream, extract the control byte and perform any required baseline wander adjustments.

2.1 Framing Requirement

Existing 100BASE-TX uses 4B5B coding in order to convey extra signaling information using the 16 additional codepoints. This implies an overhead of 25% of the MII data rate when transmitted on the line via the MDI. These additional codepoints allow the following functions to be carried :

- Data
- Start/End of Stream Delimiter (SSD/ESD)
- Error Conditions
- Idle line
- Provides DC balance

The SSD is used by the receiver to lock onto the received frame, and has the property that allows itself to be uniquely identified in a serial data stream. Once the receiver is in frame sync, the receiver determines the end of packet by searching for the ESD (unique pattern once in sync).

2.2 Transmit Framing

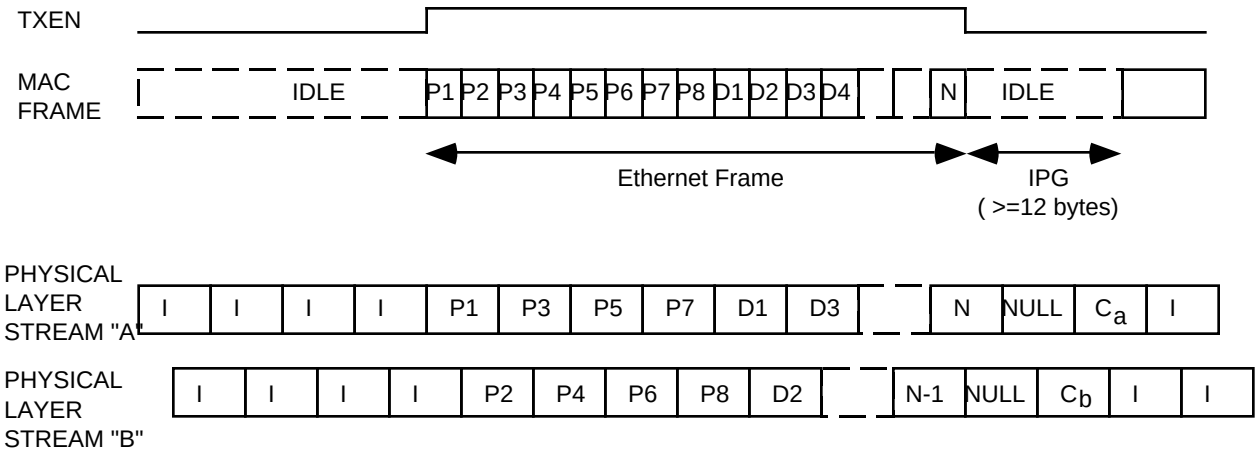
The proposed solution here uses a modified 2B1Q line coding called 4LZS which has the distinct advantage that a 2x compression of the data rate occurs, unlike 4B5B or 8B10B which actually increases the data rate by 1.25.

Start of frame will be denoted by a change from the idle pattern to the preamble pattern. At the end of the ethernet packet, a NULL will be transmitted for 4 symbol periods (1 byte), followed by a control byte. The NULL symbol implies that no signal will be driven onto the line. The receiver will be able to detect this to delineate the frame. After the EOP null, the transmitter will output a single control byte which is used to provide DC balance, and provide channel control bits.

Note that the MAC frame will be transmitted over two separate links (denoted as stream A and stream B) each having their own SOP and EOP indications. The pair division multiplexing will be done at the byte level and hence one pair will transmit the odd bytes and the other will transmit the even bytes.

In the dual (8-pair) case, 4 transmit and receive streams will exist and will be denoted stream A, B , C and D. In this case, time slicing will ensure each stream will transmit one byte in four that arrive at the GMII.

The mapping of MAC frames to physical layer streams is illustrated in Fig. 4.



Note 1 :
P1 - P8: Preamble bytes including the SFD
D1-D99: Packet data including the DA, SD, LEN and CRC
C_a: Control byte Stream A
C_b: Control byte Stream B
I: Idle byte
NULL: zero state - the transmitter turns off for 1 byte

Fig. 4 MAC Frame to Physical Layer Stream Mapping

2.2.1 Inter Packet Bytes (I, E)

When the PHY has completed transmission of the frame, it will generate inter-packet bytes. These bytes will vary depending on various conditions. Normally, after the end of packet has been denoted by a combination of the NULL and a control byte, the PHY will generate Idle bytes. This will persist until the start of the next frame. This allows the receiver to remain in bit sync, and at the same time allows the receiver to gain frame sync by checking for an idle to preamble transition. If carrier extension is required, then carrier extension bytes (E-bytes) will be transmitted after the NULL and control bytes. At the end of the carrier extension period, idle bytes will be transmitted until the start of the next frame.

For the single bundle case, the whole frame will have been split into 2 streams and the preamble sequence for stream A and stream B will be as shown below (P1 - P7 are the preamble bytes). Note that stream A always transmits the 1st, 3rd, 5th etc bytes of the frame. Similarly, stream B will transmit the 2nd, 4th etc, and hence the last byte of the split "preamble" will be the SFD byte.

Stream A "preamble":	P1 10101010	P3 10101010	P5 10101010	P7 10101010
Stream B "preamble":	P2 10101010	P4 10101010	P6 10101010	SFD 10101011

An I- byte consists of the following : 11100001

An E-byte consists of the following : 11001001

2.2.2 Control Byte (C)

The control byte will be transmitted by each stream framer at the end of the split frame, after the EOP null. Various bits within the C-byte are used for:

- DC Balance Control
- Link Control
- Link Integrity

2.3 Frame Scrambling

The entire packet excluding the control byte are scrambled using a self synchronous scrambler. This is used to contain the spectral density of the ethernet frame. The use of a self synchronizing scrambler also eliminates the possibility of a "killer packet".

2.4 Receive Framing

2.4.1 Byte Alignment

The receive framer will be receiving 2 or 4 parallel serial data streams, depending on single or dual cable implementation. Its function is to achieve frame alignment on all streams by hunting for a transition from the I-byte to the P-byte. In the single cable case, stream A may use all 4 P-bytes to achieve alignment. Stream B must use only 3 P-bytes and the SFD byte. For the dual cable case, all 4 streams will use only 2 of the P-bytes for alignment.

Due to the delay variation of each pair of UTP-5, either framer A or framer B will achieve alignment first, and therefore one framer should wait until the other framer has also received alignment. This requires buffering of some bytes prior to passing the frame up to the MAC via the GMII. By specifying the delay variation of each pair of UTP-5 for a given cable, the amount of buffering can easily be bounded. Exact operation and synchronization of the two stream framers is implementation specific. The two framing state machines will communicate so as to provide the correct byte

multiplexing of the two streams. It is defined that stream A transmits first, followed by stream B, but the streams may well be received in a different order.

Once both framers are in sync, the frame is regenerated from the two byte streams and passed up to the MAC layer via the GMII.

2.4.2 End of Packet Delineation

The end of frame is detected by each framer by waiting for the null on the line, followed by a control byte. When the receiver detects this condition, the end of packet is reached. The receiver will now be in an idle condition, waiting to detect an idle to preamble transition for detection of the next packet.

The RX_DV signal to the MAC will be controlled based on the total length of the assembled packet from the two steams.

2.5 Serial to Parallel Conversion

In the transmit path, the bytes being transmitted by each framer at 62.5Mbytes/s will be serialized to form two streams each at 500Mbps. Similarly in the receive path, two serial 500Mbps streams will be converted to 62.5Mbytes/s streams by the receive framer.

2.6 4LZS Coding (2B1Q with zero state)

The proposed coding scheme allows for a 2x compression of the line rate. 2B1Q line coding maps 2 bits into one of 4 possible levels. The addition of a zero state allows the detection of the end of the frame by the receiver.

The mapping of the bits into symbols, and subsequent voltage levels are illustrated below:

Bits	Symbol	Level (mv)
10	+3	450
11	+1	150
NULL	0	0
01	-1	-150
00	-3	-450

2.6.1 Comparison of 4LZS against NRZ

The spectral shape of a 4LZS line code compared with an NRZ line code is illustrated in Fig. 5 below:

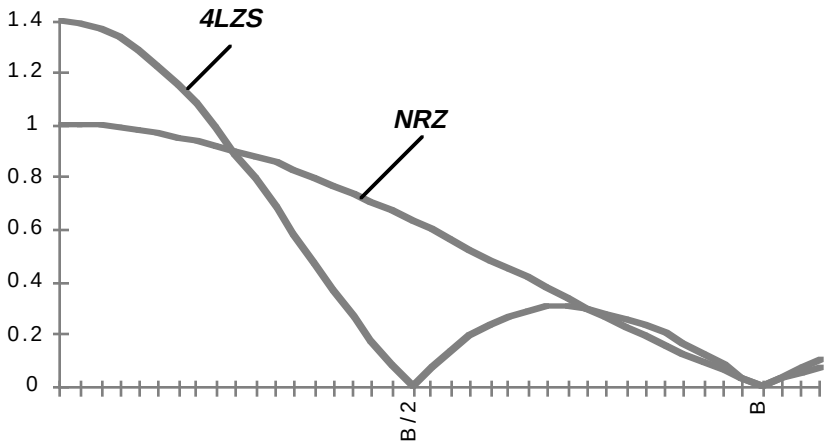


Fig. 5 Spectrums of 4LZS and NRZ Line Codes

The resulting ideal eye diagram of a 4LZS line code is shown in Fig. 6 below.

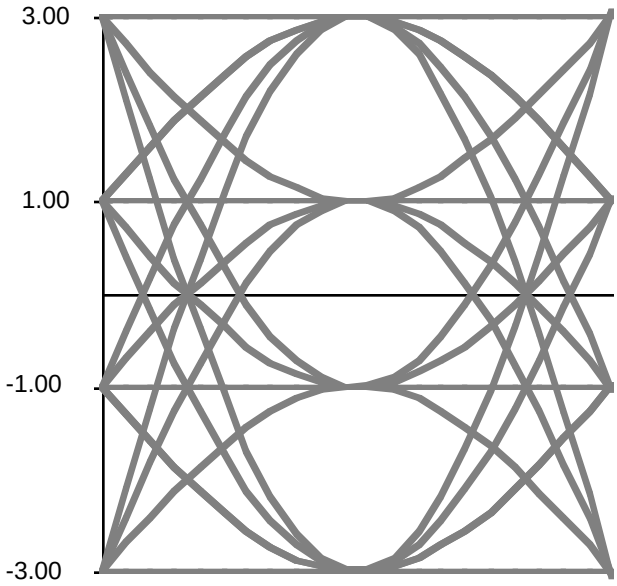


Fig. 6 Ideal 4LZS Eye Diagram

2.6.2 Theoretical Analysis of 2B1Q against NRZ

Additional SNR required at the slicer may be computed as the intrinsic coding power density, which is the "symbol variance":

$$SNR = \sigma^2_s / \sigma^2_n \; ; \; \Delta SNR = \sigma^2_{s2B1Q} / \sigma^2_{sNRZ}$$

where, $\sigma^2_s = 1/L_c \sum_i \langle e_i^2 \rangle$

$$\sigma^2_{s2B1Q} = 1/4 \{ (-3)^2 + (-1)^2 + (1)^2 + (3)^2 \} = 5$$

$$\sigma^2_{sNRZ} = 1/2 \{ (-1)^2 + (+1)^2 \} = 1$$

Therefore,

$$\Delta SNR = \sigma^2_{s2B1Q} / \sigma^2_{sNRZ} = 10\log(5/1) = \mathbf{7dB}$$

In addition to the SNR penalty at the receiver, noise and loss are proportional to the symbol period and cable geometry.

Flat channel noise power is proportional to the symbol rate (1/T) :

$$\Delta\sigma_{nflat} = -10 \log [T_{2B1Q} / T_{NRZ}]$$

$$= \mathbf{2\ dB} \text{ @ 250Mbaud vs 155Mbit NRZ}$$

Self NEXT noise power is proportional to the cubed square root of the symbol rate ($T^{3/2}$) :

$$\Delta\sigma_{nsnext} = -15 \log [T_{2B1Q} / T_{NRZ}]$$

$$= \mathbf{3\ dB} \text{ @ 250Mbaud vs 155Mbit NRZ}$$

NEXT noise power is frequency and cable geometry dependent :

$$N(f) = \chi f^{3/2} G(f) \; ; = \chi = 6.31 \times 10^{-7} \text{ for UTP5}$$

$$= \mathbf{3\ dB} \text{ @ 250Mbaud vs 155Mbit NRZ}$$

In summary, 250Mbaud 2B1Q penalties over 155NRZ are:

6dB attenuation,
2dB flat channel noise,
3dB self NEXT,
3dB pair-pair NEXT
7dB at the slicer

Totaling a **21dB** penalty. But how far is 21dB?

Characterizing power spectral density at the centre frequency:

$$NRZ(155) \sim 1.967\sqrt{f} + 0.023f + 0.05/\sqrt{f} = 19.1 \text{ dB/100m @ 77.5 MHz}$$

For 2B1Q (dB/100m) x D metres = NRZ (dB @ 100m)

$$D = 19.1 / (19.1 + 21) = 48 \text{ metres}$$

Therefore, theoretical performance:

100m of 155 NRZ = 48m for 250Mbaud/pair 2B1Q

2.7 Receiver Line Equalization

At the receiver, line equalization will be required in order to compensate for the line characteristics. This may be done using either adaptive or fixed equalization. The exact method chosen will be implementation specific and is not discussed further here.

2.8 Single or Dual Cable Operation

As mentioned earlier in this paper, an increase in the distance (or even speed) objectives is possible using dual cables having a total of 8-pairs of UTP-5.

In this scenario, each cable (of 4-pairs) would equally share the bandwidth, both cables having 2 transmit and 2 receive pairs.

An illustration of the distance/rate trade-off for both single and dual cable cases is illustrated in Fig. 7 below.

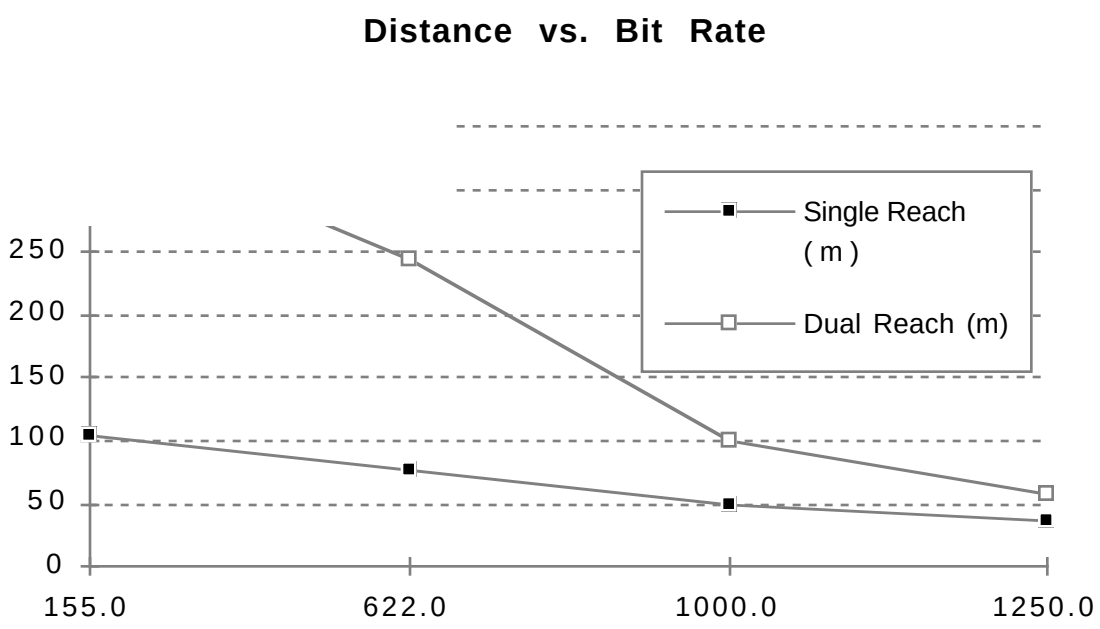


Fig. 7 Illustration of Speed vs Distance for Single/Dual 4-pair Cables

2.9 Gigabit Media Independent Interface (GMII)

The function of the GMII is to interface the PHY layer device to a higher layer function (MAC layer, via a reconciliation layer). The GMII defined here is a simple extension to the existing MII as defined in IEEE802.3u for 100BASE-X. The only significant change is the requirement to transfer 1Gbps full duplex over this interface, which using the existing nibble based interface would clearly not be practical as it would require a 250MHz clock.

The proposal here is to extend the nibble interface to a byte wide interface. This would allow 1Gbps full-duplex support using a 125MHz clock, which simplifies the required interface and allows implementation using relatively easily available technology. An additional clock is also required for retiming of the transmit data signals. This is described later.

Key features of this interface are :

- Capable of supporting 10, 100, or 1000 Mbps data rates.
- Data and delimiters synchronous to clock.
- Independent 8-bit wide transmit and receive data paths (drops back to nibble based interface for 10 and 100 Mbps).
- Uses TTL signal levels compatible with common digital ASIC CMOS processes.
- Provides simple management interface.

2.9.1 GMII Functional Overview

The following signals are required to implement the GMII. The main enhancements are signals to extend the transmit and receive nibble based interface to a byte wide interfaces (TXD and RXD). An additional output clock (TX_CLKO) is also provided by the MAC which would be retimed to the TXD signals to reduce any output jitter. This clock would be regenerated from a reference provided by the PHY layer (TX_CLKR). The complete GMII signals are:

TX_ER	RX_ER	CRS
TX_EN	RX_DV	COL
TX_CLKO	RX_CLK	MDC
TXD[7:0]	RXD[7:0]	MDIO
TX_CLKR		

In common with the MII, TX_ER, TX_EN and TXD are synchronous to TX_CLKR (TX_CLK in the MII). Similarly, RX_ER, RX_DV and RXD are synchronous to RX_CLK. CRS and COL are asynchronous to all clocks. It is proposed that the flow through clocks are defined at the GMII. That is, the PHY device would generate the RX_CLK, whereas the MAC layer device would generate the TX_CLKO.

The concept of flow through timing is illustrated in Fig. 8 below:

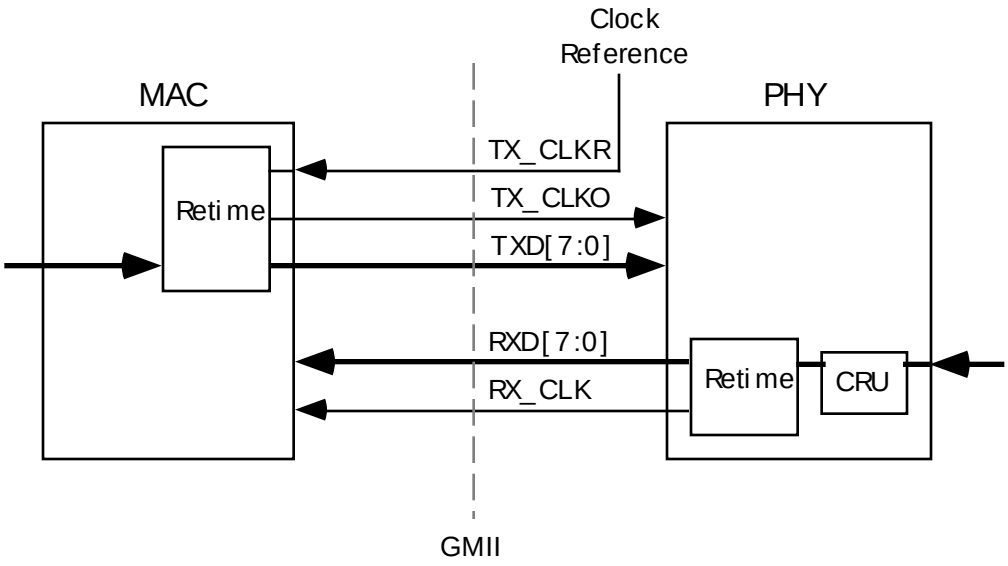


Fig. 8 Flow Through Timing at the GMII

2.9.2 GMII Functional Timing

The functional timing of the GMII is identical to that for the existing MII for 100BASE-X (TX_CLKR would be the same as TX_CLK). This is shown for both transmit and receive paths in Fig. 9 and Fig. 10 below. Note that CRS and COL are shown simply to indicate the asynchronous nature of the signals and should not necessarily be read in conjunction with the other waveforms :

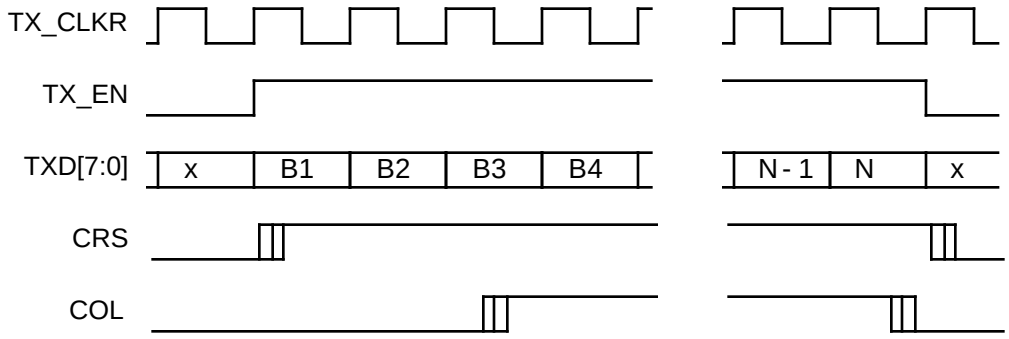


Fig. 9 GMII Transmit Timing

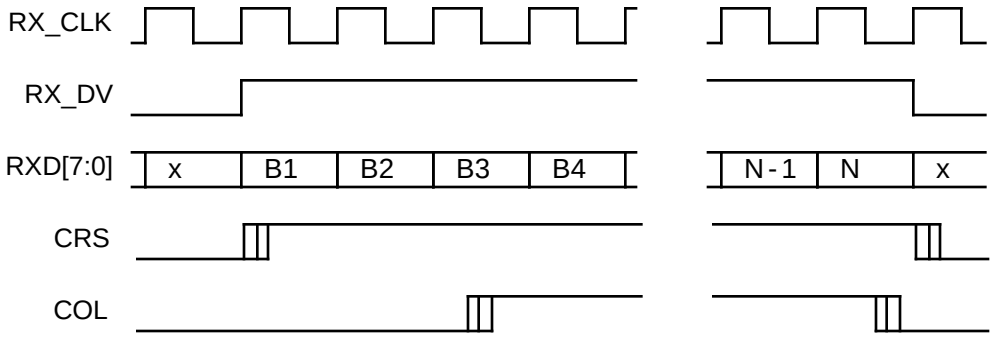


Fig. 10 GMII Receive Timing

2.9.3 GMII AC Timing

The AC timing and drive requirements for the GMII will be different from MII. With a receive and transmit clock frequency of 125MHz, the period is 8ns. Suitable propagation (T_{PD}), setup (T_{HD}) and hold (T_{SU}) times for synchronous signals across this interface are defined below:

Synchronous to TX_CLKR: (TX_ER, TX_EN, TXD[7:0])
T_{PD} = TBD
T_{HD} = TBD
T_{SU} = TBD

Synchronous to RX_CLK: (RX_ER, RX_DV, RXD[7:0])
T_{PD} = TBD
T_{HD} = TBD
T_{SU} = TBD

This is illustrated in Fig 11 below:

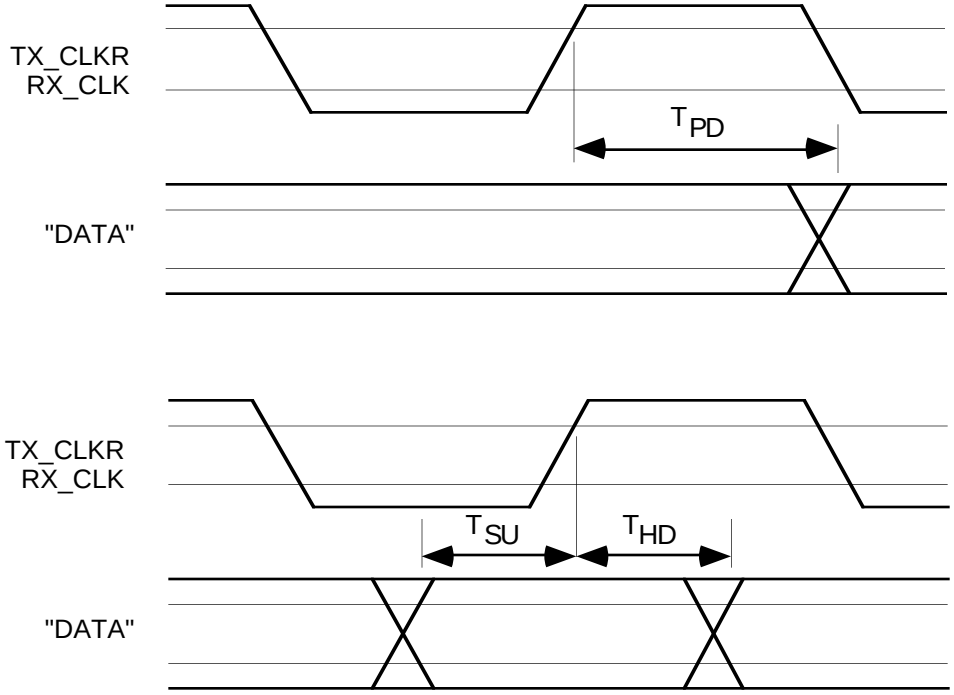


Fig. 11 GMII AC Timing Characteristics

2.9.4 GMII Management Interface

MDC and MDIO are used to provide a management interface. Control register 0 and Status register 1 are referred to as the "basic register set". Bits would need to be defined in both of these registers to control/indicate 1Gbps support. The functionality of the interface is unchanged except for the addition of these registers.

3. Simulation Model and Results

3.1 Overview

Characterization of UTP-5 cable was performed from (DC) to 300 MHz. Using a step input, several different samples of both Belden "DataTwist-5" and AT&T "Systemtwist" 1061B were measured at lengths of 0, 20, 40, 60, 80, 100 and 120 meters. Polynomial curve fitting of the measured data was performed using the MATLAB "Polyfit" function. The worst case error of the polynomial against measured data was less than 0.1%. Using MATLAB, the step response polynomials were transformed to the frequency domain in order to obtain the UTP-5 cable transfer function (magnitude and phase vs frequency) for each cable length.

Two 4-level stimulus functions were generated assuming a 30% UI (1.2 ns in a 4.0 ns period) edge interval. The two different stimulus functions cover all transitions and resulting trajectories and are DC balanced. No allowance for baseline wander was included. The time domain stimulus functions were transformed to the frequency domain using the MATLAB "FFT" function.

Using the cable transfer function for various cable lengths and the 4-level frequency domain stimulus, the cable response as a function of length was generated. This result was transformed back to the time domain. (The MATLAB inverse function was used.) Eye diagrams were generated by superimposing each of the transitions of the time domain results.

An unequalized eye generated from a simulated 20m cable is illustrated in Fig 12.

The simulation results were promising enough to believe that a physical prototype would be worth investigating. This work is described next.

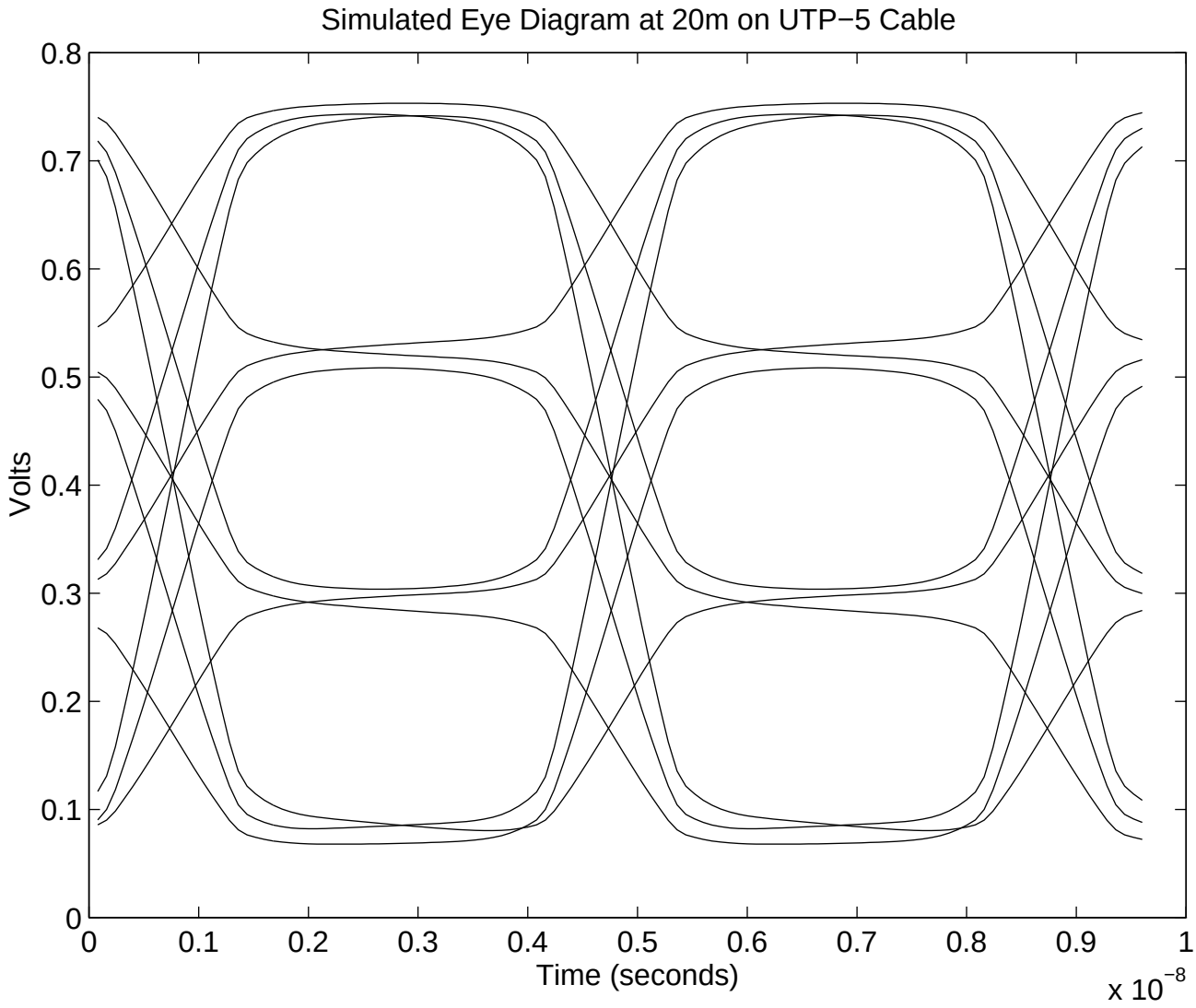


Fig. 12 Simulated Eye Diagram at 20m on UTP-5 Cable

4. Hardware Evaluation and Results

4.1 Overview

A discrete implementation of the PMD discussed in this proposal was built to analyze the performance and behavior of the proposed method, and observe the eye opening under realistic conditions.

A simplified block diagram of the evaluation board is shown in Fig. 13 below:

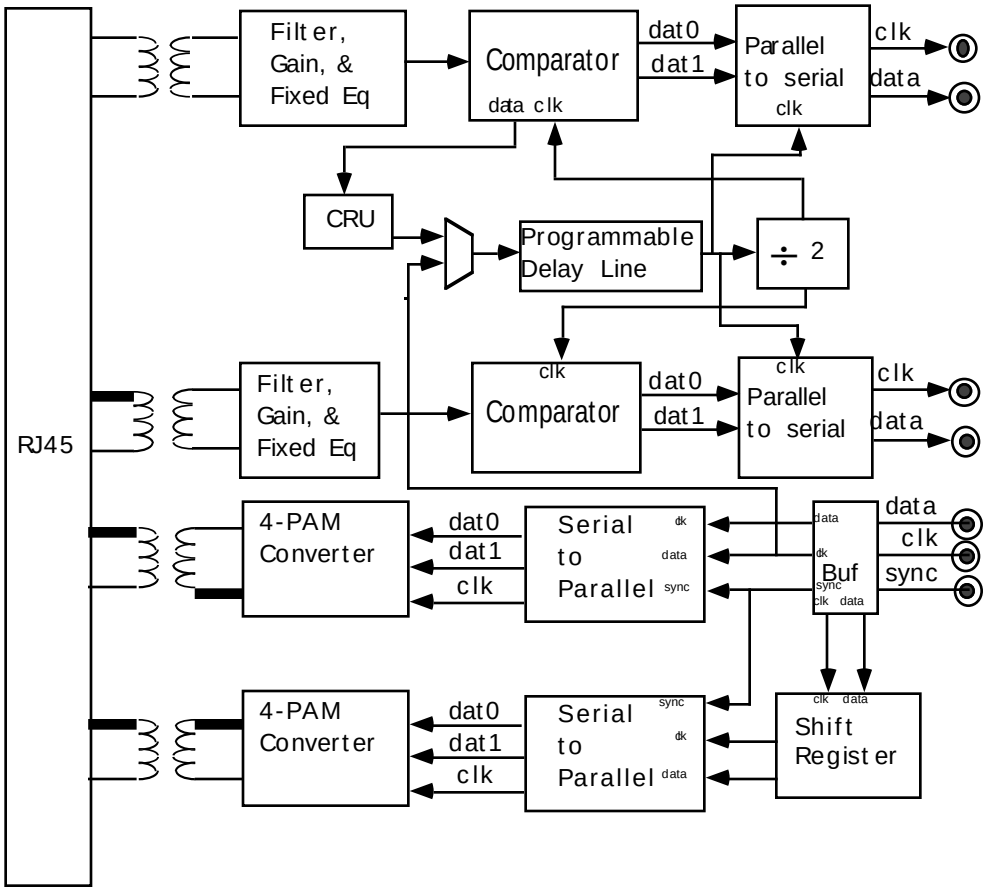


Fig. 13 PMD Evaluation Board Block Diagram

Features of the eval board are:

- 2 transmit and 2 receive channels for NEXT measurements (self, pair-pair, far)
- Each channel operates at 500+ Mbps
- Discrete equalizer

4.2 Test Configuration

Various tests were performed while transmitting a 1Gbps serial data stream from a BER Tester and observing the received eye diagram over various cable lengths. No line equalization at the receiver was performed on any of these tests.

Two different configuration were used.

Configuration 1 uses only the transmit section of the evaluation board. The eyes are observed after some defined length of cable, plus 2 x 3m patchcords. Test configuration 1 is illustrated in Fig. 14.

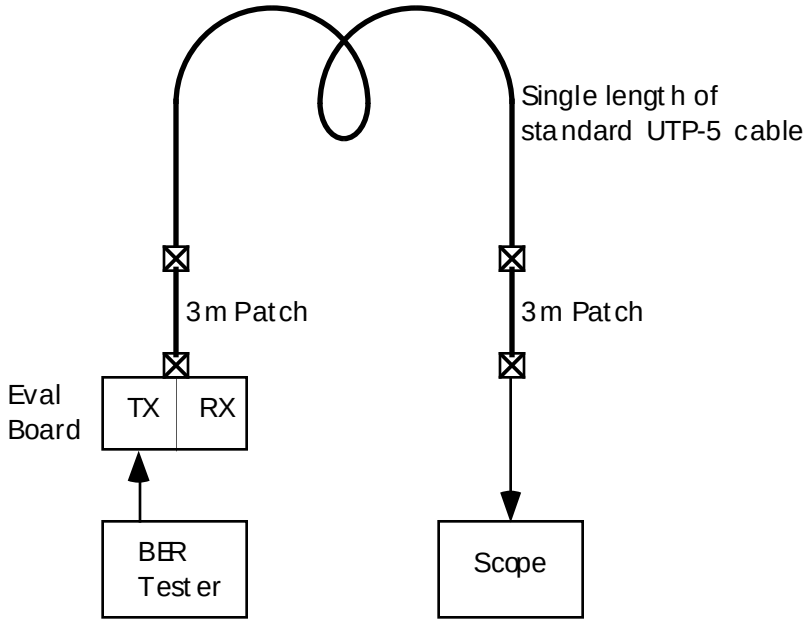


Fig. 14 Test Configuration 1

Configuration 2 uses both the transmit and receive sections of the evaluation board. The eyes are observed after some defined length of cable, plus 2 x 3m patchcords. In addition, the eyes are observed at the output of the receive pre-amplifier. Test configuration 2 is illustrated in Fig. 15.

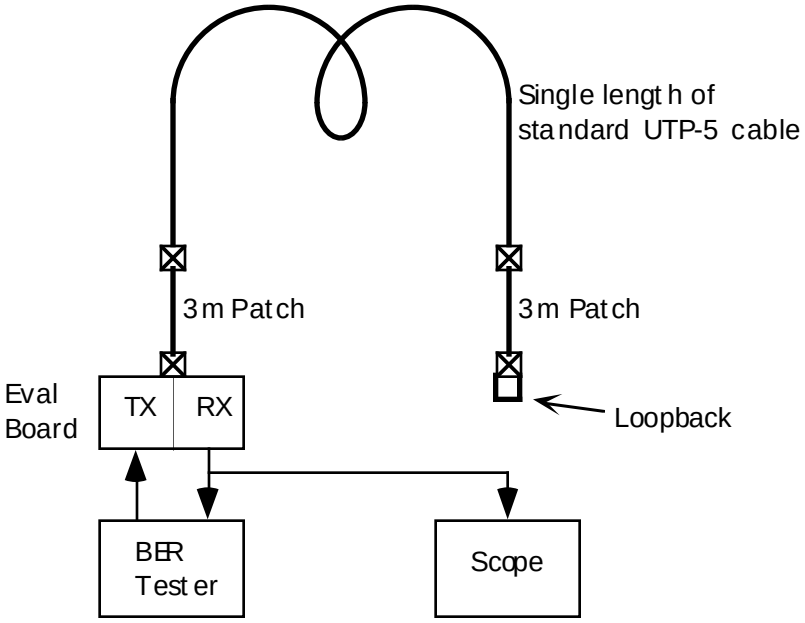


Fig. 15 Test Configuration 2

4.3 Test Procedure

Tests were run using varying cable lengths from 2 major suppliers of UTP-5 cable (AT&T Systimax 1061B, and Belden Datatwist-5 1583A).

The BER tester was used to provide 3 different data patterns (fixed, PRBS-7 and PRBS-23).

The individual tests are illustrated in the following table:

Test Num	Test Config	Test Pattern	Line Equalization	Horizontal Distance	Eye Plot
T1	1	PRBS-23	No	3	Plot 1
T2	1	Fixed (36H)	No	20	Plot 2
T3	1	PRBS-23	No	20	Plot 3
T4	1	PRBS-7	No	20	Plot 4
T5	1	PRBS-23	No	30	Plot 5
T6	2	PRBS-7	No	26	Plot 6

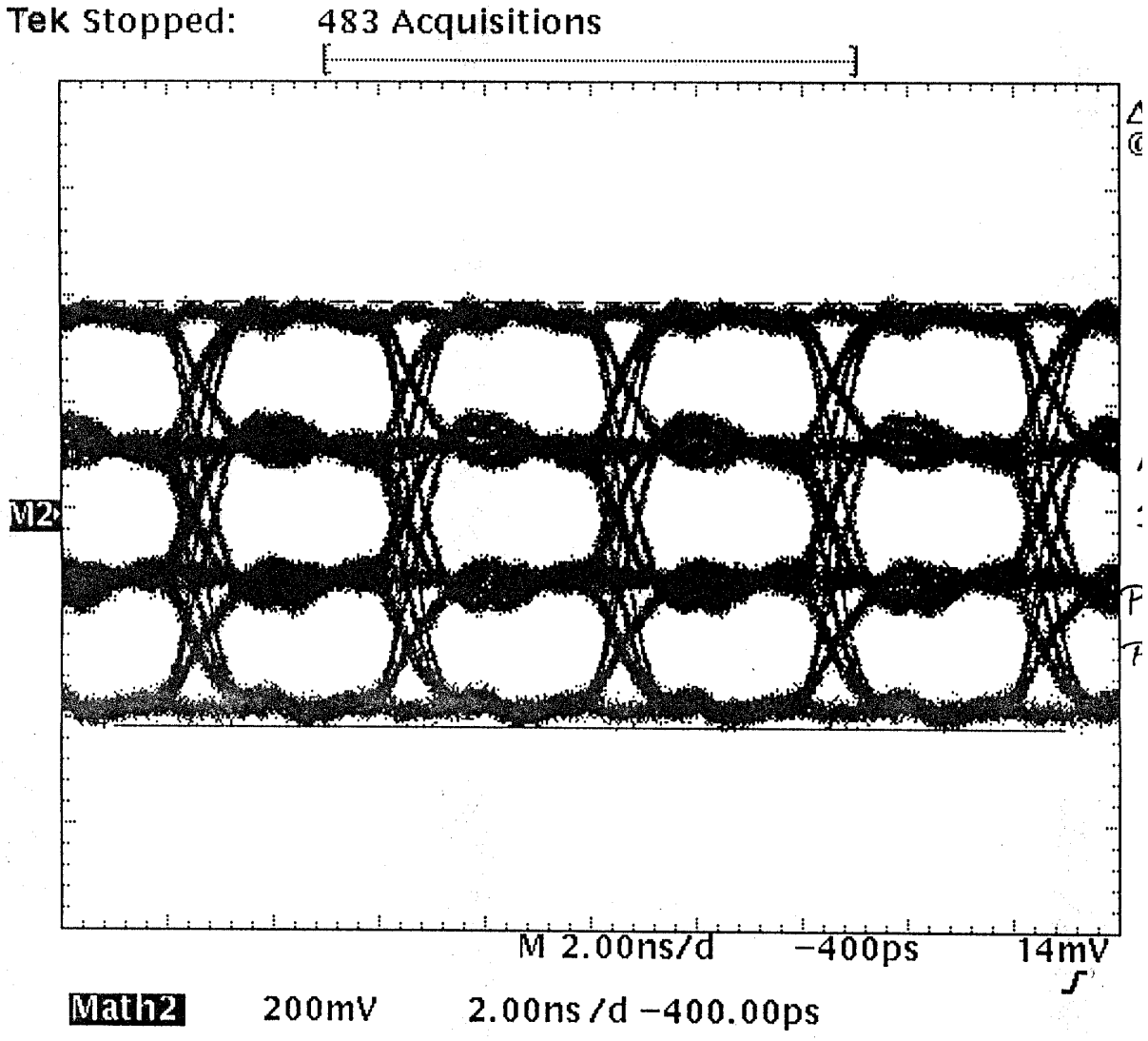
4.4 Test Results

The resulting eye diagrams for the test described above are shown in Plots 1 -6.

Plot 6 illustrates the eye measured at the output of the receive pre-amplifier, but with no line equalization. For this test configuration, a BER test was performed using a PRBS 7 pattern, running over 26m of cable and 6m of patch. This test ran error free for 15 minutes. This translates to a BER of 10^{-7}.

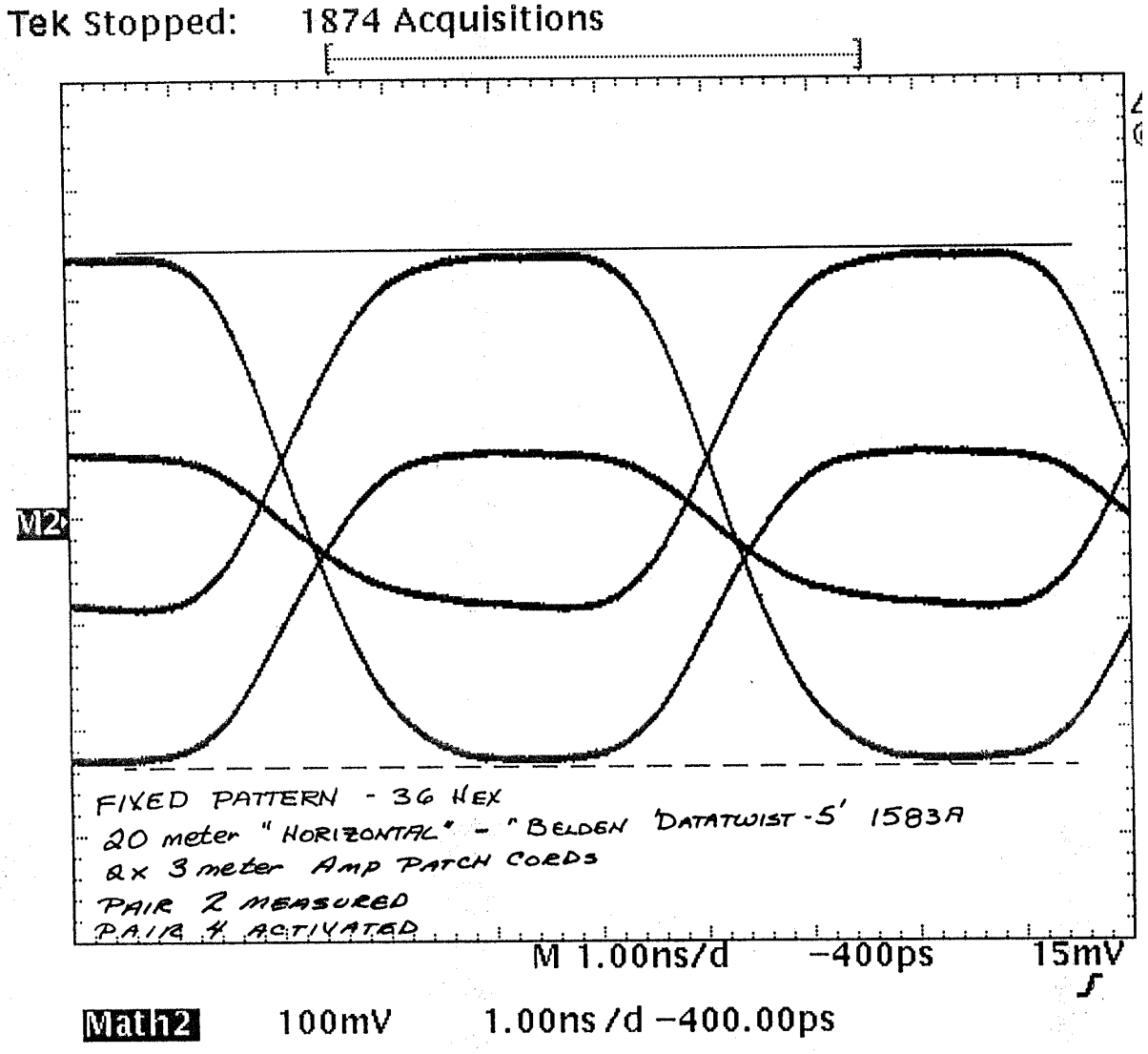
Plot 1:

PRBS 2^{23} - 1
3m "Horizontal" Belden Datatwist-5 1583A.
2 x 3m AMP patch cord.
Pair 2 measured.
Pair 4 activated.
(10µF AC coupling @ scope)



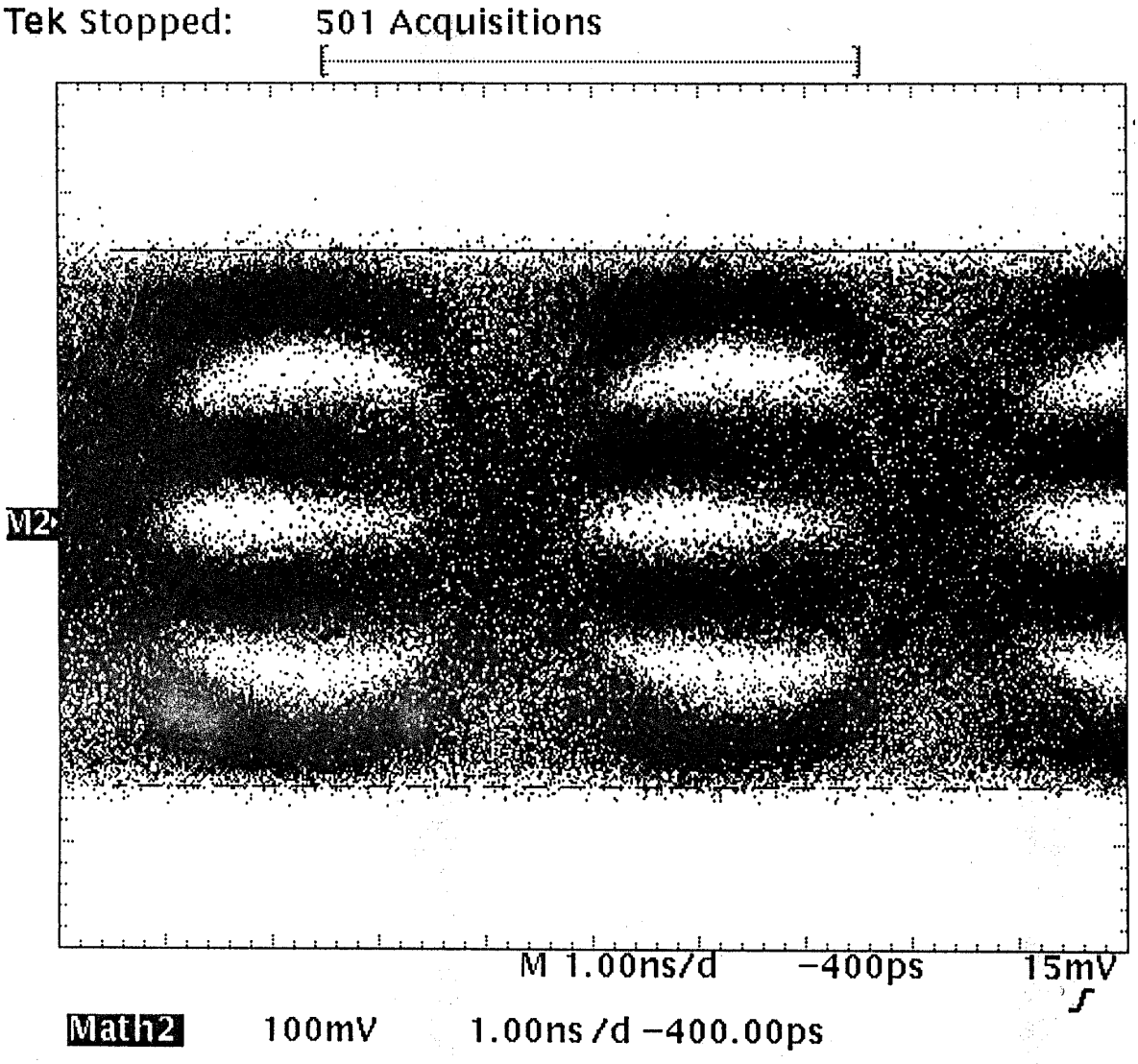
Plot 2:

Fixed Pattern (36 hex).
20m "Horizontal" Belden Datatwist-5 1583A.
2 x 3m AMP patch cord.
Pair 2 measured.
Pair 4 activated.



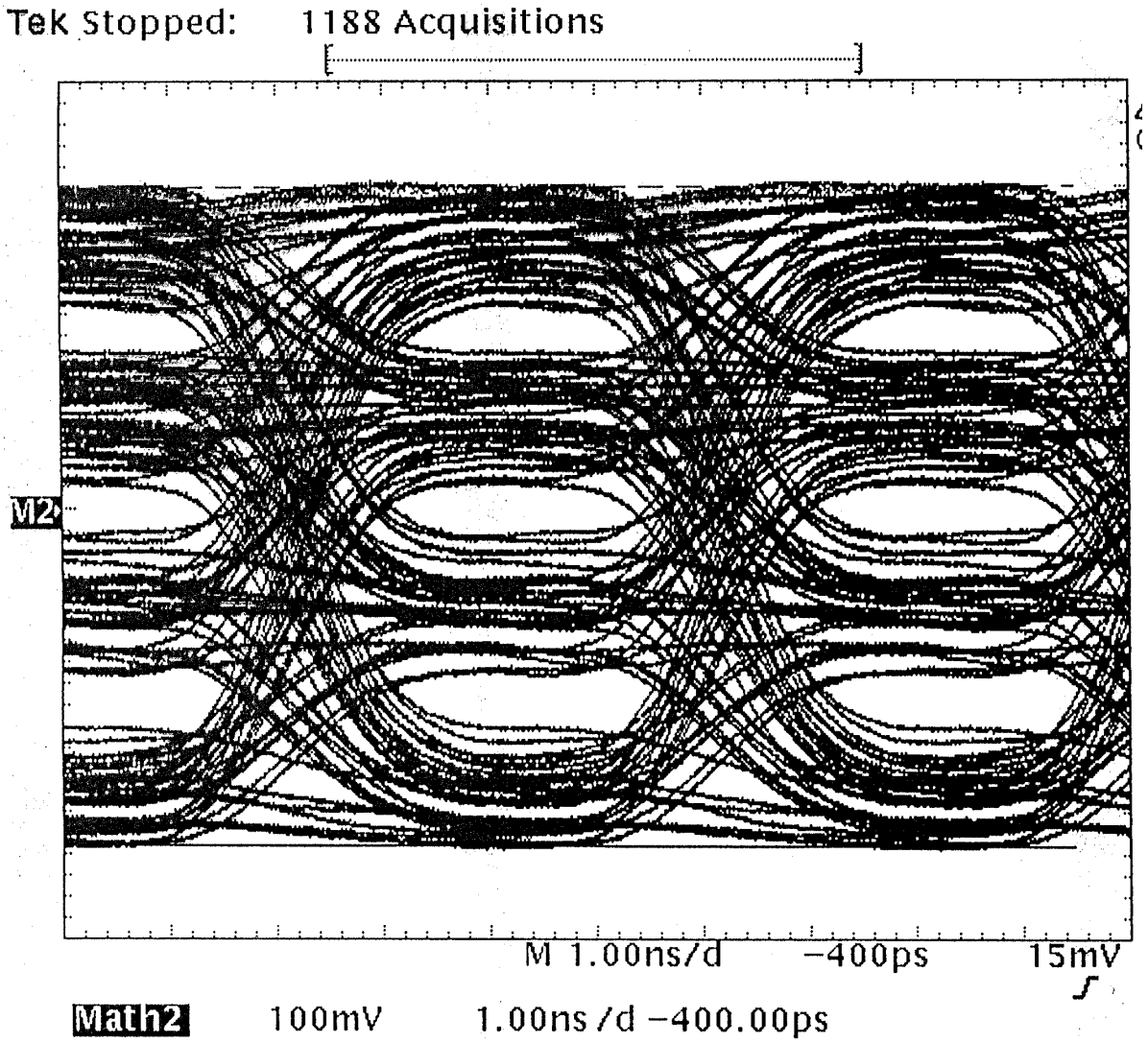
Plot 3:

PRBS $2^{23} - 1$
20m "Horizontal" Belden Datatwist-5 1583A.
2 x 3m AMP patch cord.
Pair 2 measured.
Pair 4 activated.



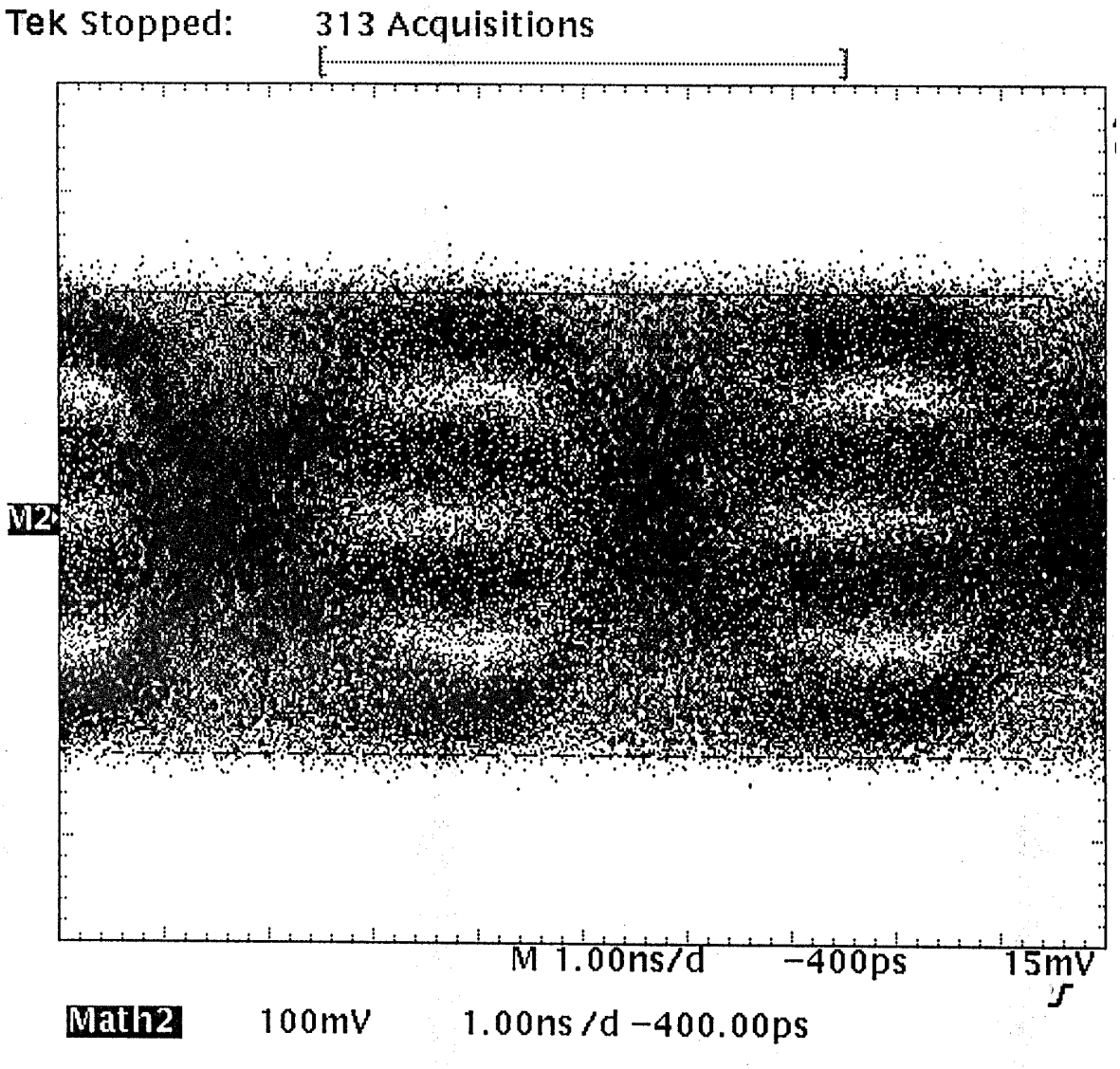
Plot 4:

PRBS 2^7 - 1
20m "Horizontal" Belden Datatwist-5 1583A.
2 x 3m AMP patch cord.
Pair 2 measured.
Pair 4 activated.
(0.1µF AC coupling @ scope)



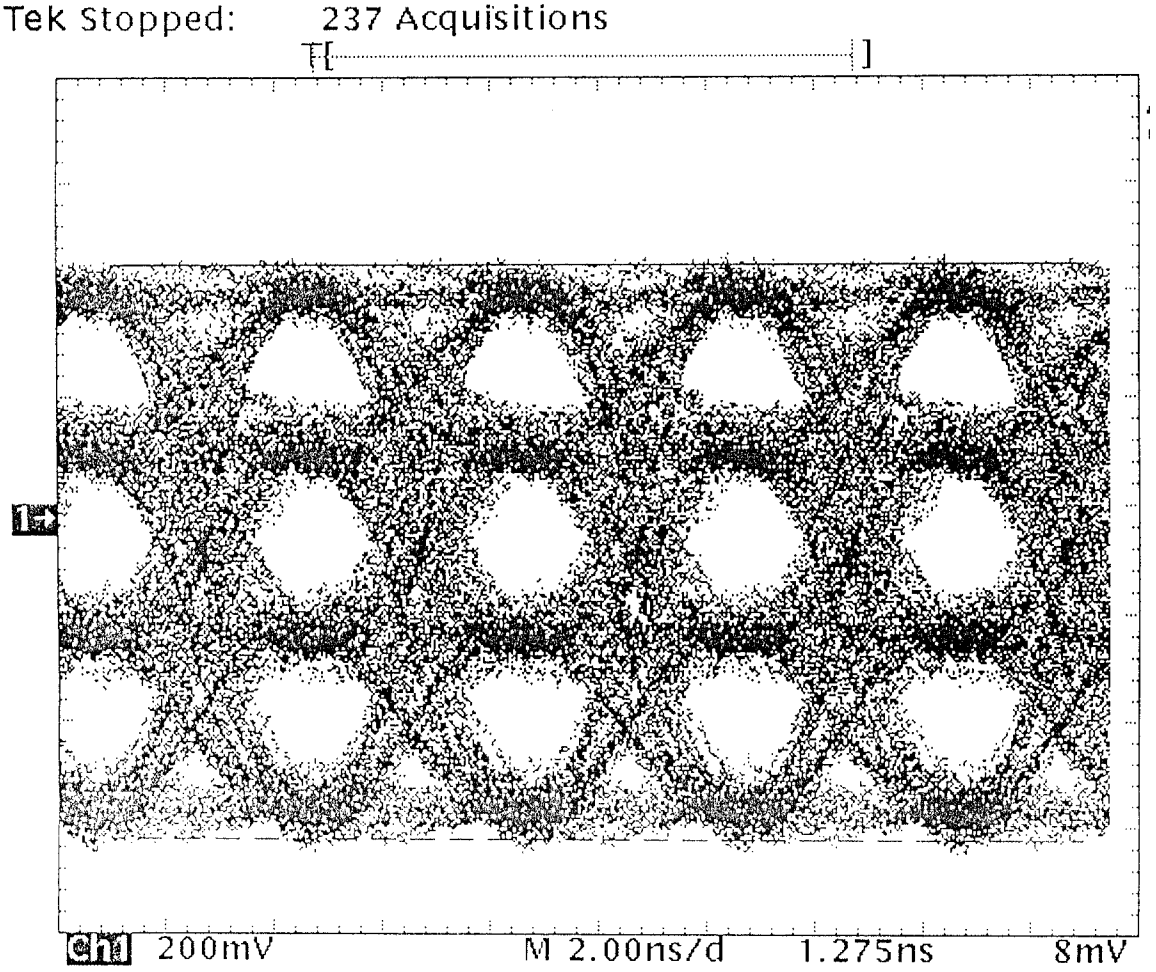
Plot 5:

PRBS 2^{23} - 1
30m "Horizontal" AT&T Systimax 1061B.
2 x 3m AMP patch cord.
Pair 2 measured.
Pair 4 activated.
Pulse PE-65508 transformers.
(0.1µF AC coupling @ scope)



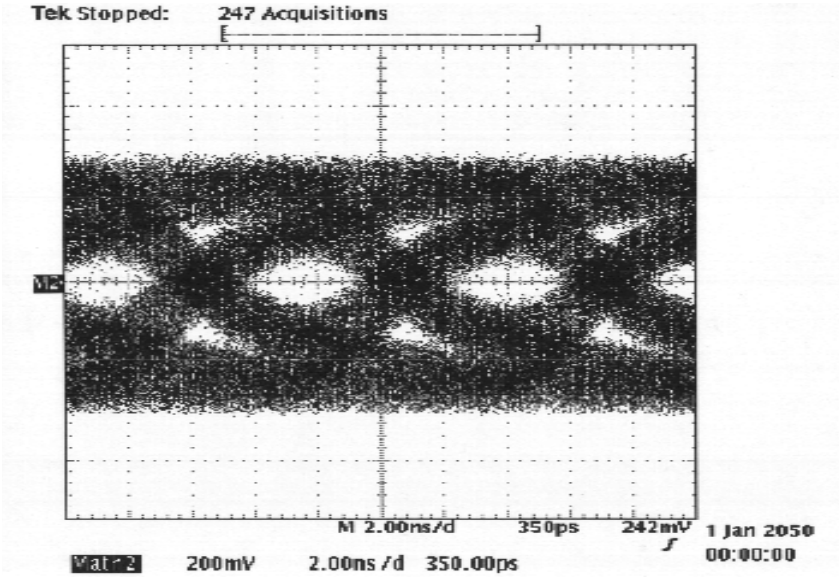
Plot 6:

PRBS 2^7 - 1
26m "Horizontal" AT&T Systimax 1061B.
2 x 3m AMP patch cord.
Pair 2 activated.
Pair 4 activated.
Monitored after receive pre-amplifier.
No implicit line equalization.

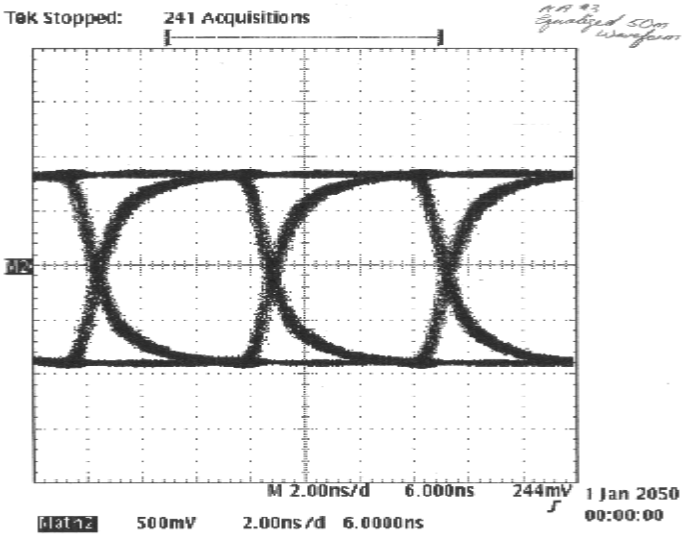


4.4 Effect of Line Equalization

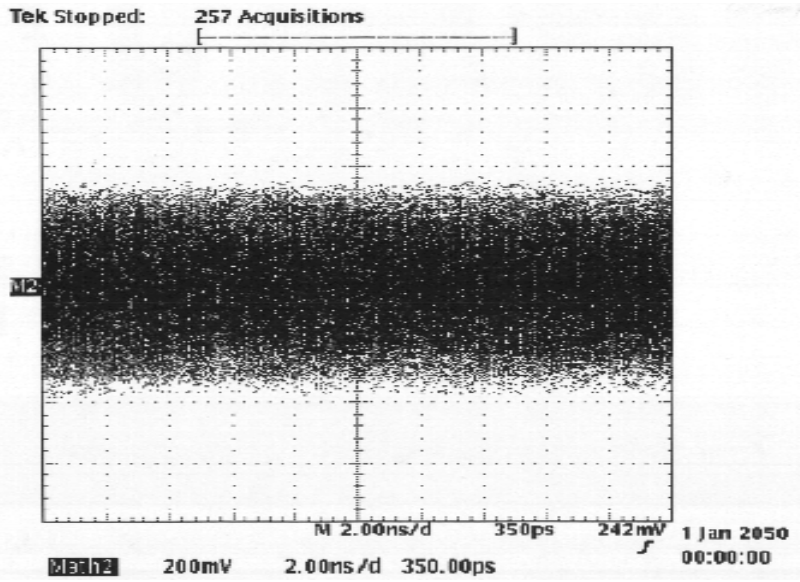
The eye diagrams illustrated in plot 1 -6 do not use any kind of line equalization at the receiver. To illustrate the performance when line equalization is used, the following plots show the improvement of the received eyes for various cable lengths. These results were obtained by measuring 155.52Mbps Non-Return Zero (NRZ) over UTP-5.



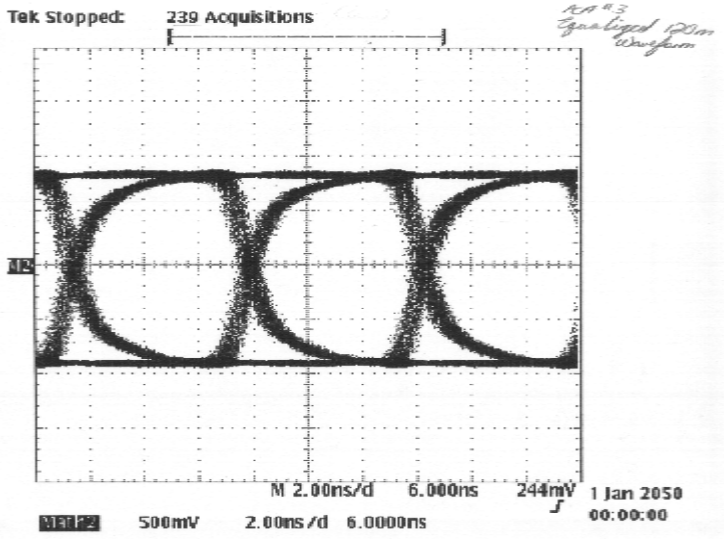
Plot. 7 Unequalized after 50m of UTP-5 @ 155Mbps NRZ



Plot. 8 Equalized after 50m of UTP-5 @ 155Mbps NRZ



Plot. 9 Unequalized after 120m of UTP-5 @ 155Mbps NRZ



Plot. 10 Equalized after 120m of UTP-5 @ 155Mbps NRZ

As can be seen from the above plots, the use of line equalization dramatically improves the recovered eye from what appears at first to be an unrecoverable signal.

5. Conclusion

In this report we have detailed a method for transmitting 1Gbps full duplex ethernet frames over a single UTP-5 cable bundle (4 pairs) using a 4LZS signaling scheme. Ethernet frame start and end delineation is possible using idle/preamble detection and null state detection.

Empirical results were shown to demonstrate that acceptable performance could be achieved (BER < 10^{-10}) over distances of 50m. These empirical results were also correlated with simulation results.

This method also lends itself for data transmission over longer distances or even higher rates using 2 cables containing a total of 8 pairs of UTP-5. Using 2 identical implementations operating in parallel, operation at 1Gbps using 2 cables would be achievable at distances of more than 100m.

Work for further study include the following:

- BER performance over temperature.
- Spectral and FCC measurements.
- DC Balance requirements (decision feedback at receiver verses transmitter running digital sum correction).
- Requirement for "Escape" words (error conditions, transparent signaling channels).
- Transmit templates and slicing levels.

6. References

[1] IEEE802.3u, "MAC Parameters, Physical Layer, Medium Attachment Units, and Repeaters for 100 Mbps Operation , Type 100BASE-T"

[2] IEEE802.3x, "Specification for 802.3 Full-Duplex Operation"

[3] EIA/TIA-568-A Standard, "Commercial Building & Wiring Telecommunications Wiring Standard", Letter Ballot, 1994.

[4] J.J. Werner, "Tutorial on Carrierless AM/PM - part II", ANSI X3T9.5 TP-PMD submission, Austin, Feb1993.

[5] T. Banwell, W. Stephens, "Line Code Selection for 155.52Mbps Data Transmission on Catagory 5 Cable Plant", IEEE JSAC, Vol 13, No. 9, Dec 1995.