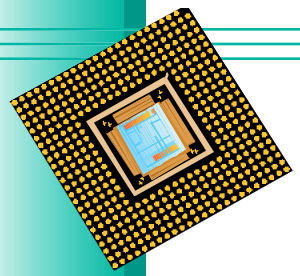

MII For Gigabit Ethernet

Jacob Twersky

Digital Equipment Corporation (Digital)

IEEE 802.3z Task Force

September 1996

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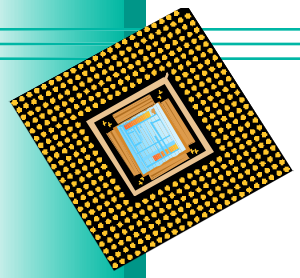
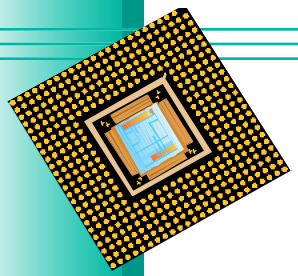


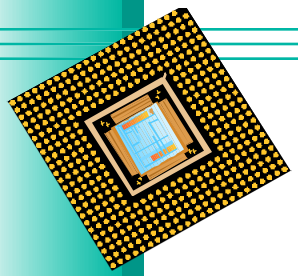
Scope

- Why Gigabit MII
- MII in the layers model and the defined interface for 10/100 Mb/s (802.3u)
- Gigabit MII proposal



Objectives

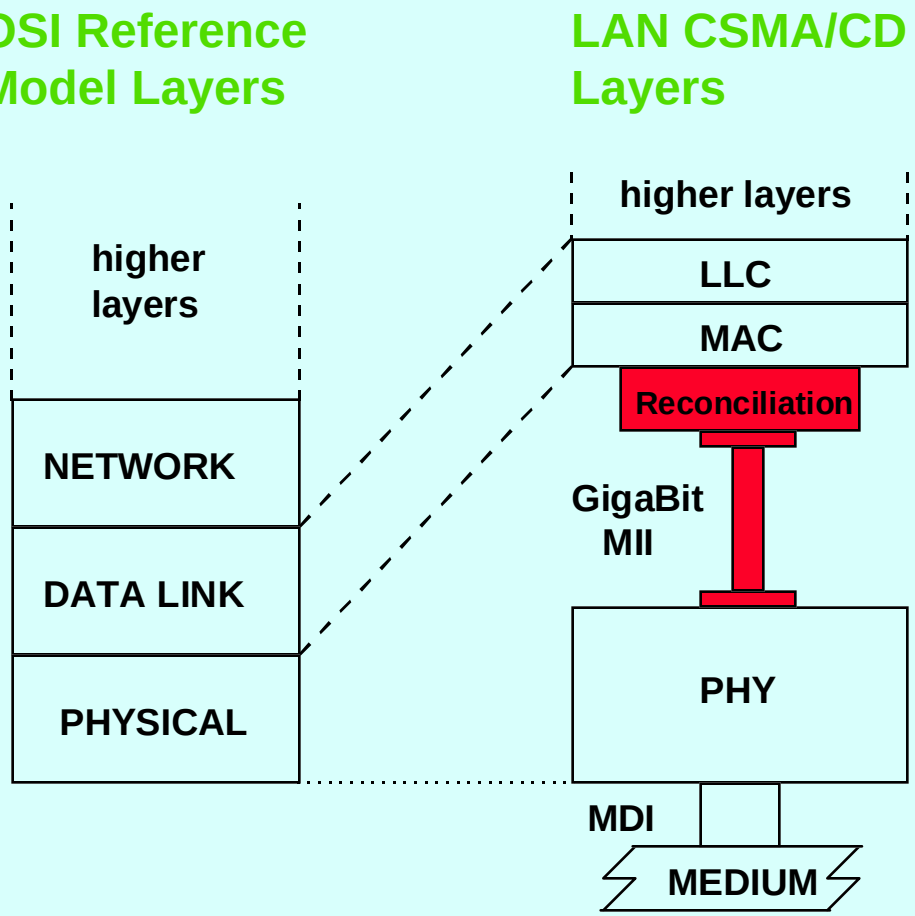
- **Logical** MII definition for Gigaethernet (no electrical and mechanical characteristics for now)
- Simple, inexpensive, easy-to-implement interconnection between PHY and MAC
- As close as possible to the 10/100 MII definition
- Allow half-duplex and full-duplex operation modes
- Extendible



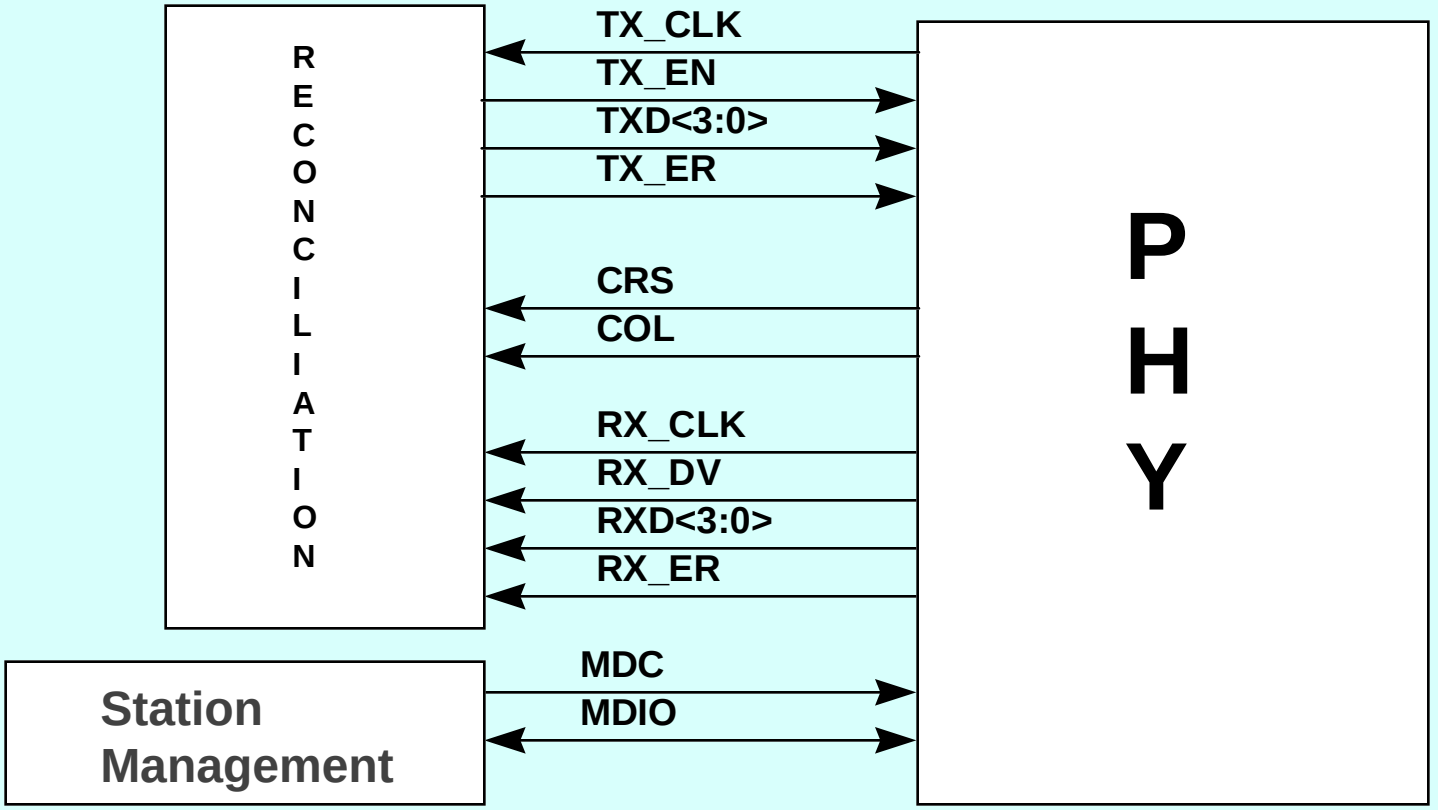
Why MII?

- Two device - MAC and PHY - implementations
  - MAC and PHY technologies may be different
  - Vendors expertise
- System vendors can choose PHYs from different chip suppliers (even for the same media)
- Makes differences among the various media absolutely transparent to the MAC sublayer
  - Identical MAC devices may be used with any media
  - MAC sublayer definition in the standard is unified

MII Within the LAN Layers Model



MII Signals in 802.3u



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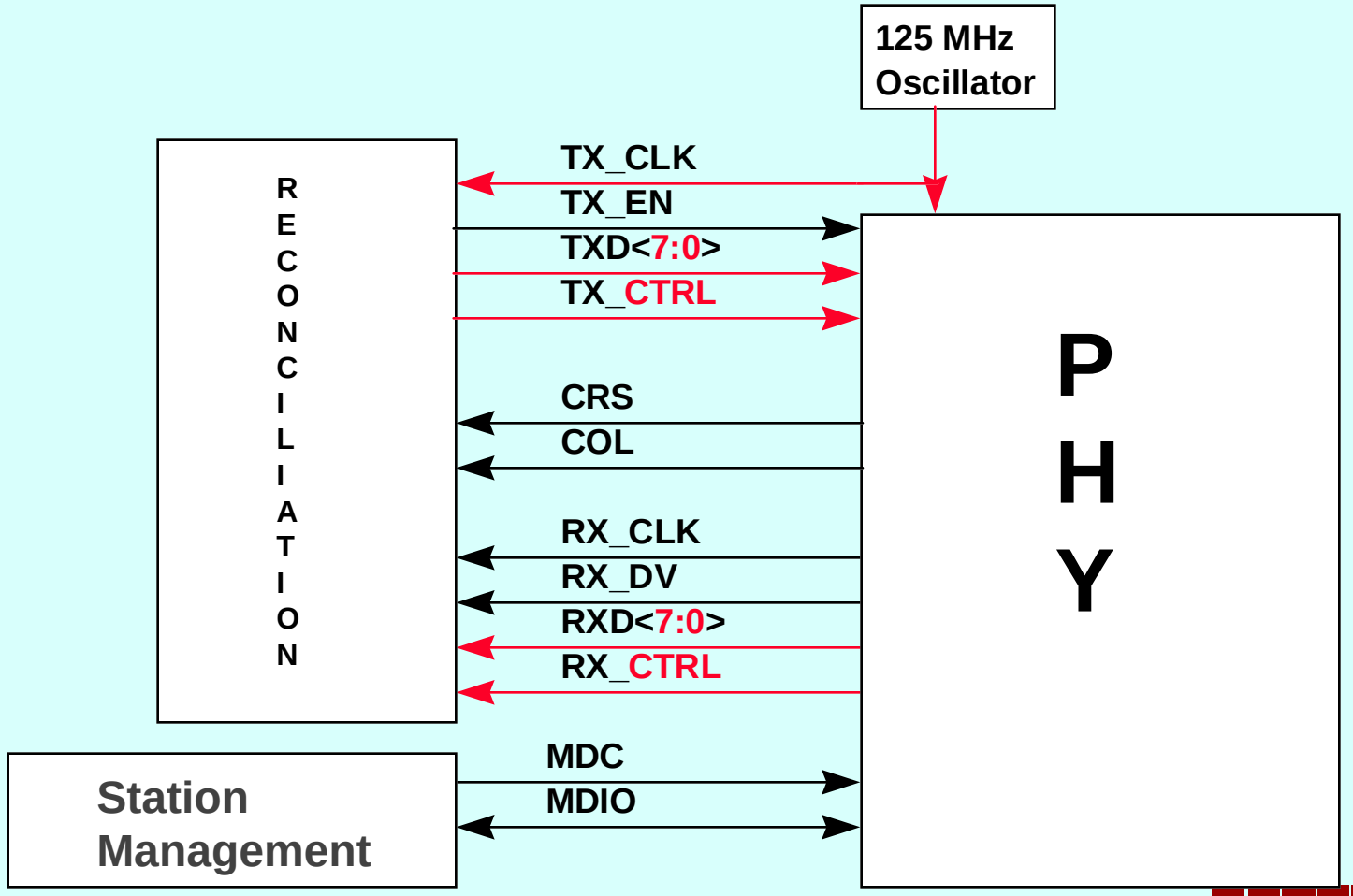
MII Signals in 802.3z



Gigabit MII - Permissible Encoding in Transmit

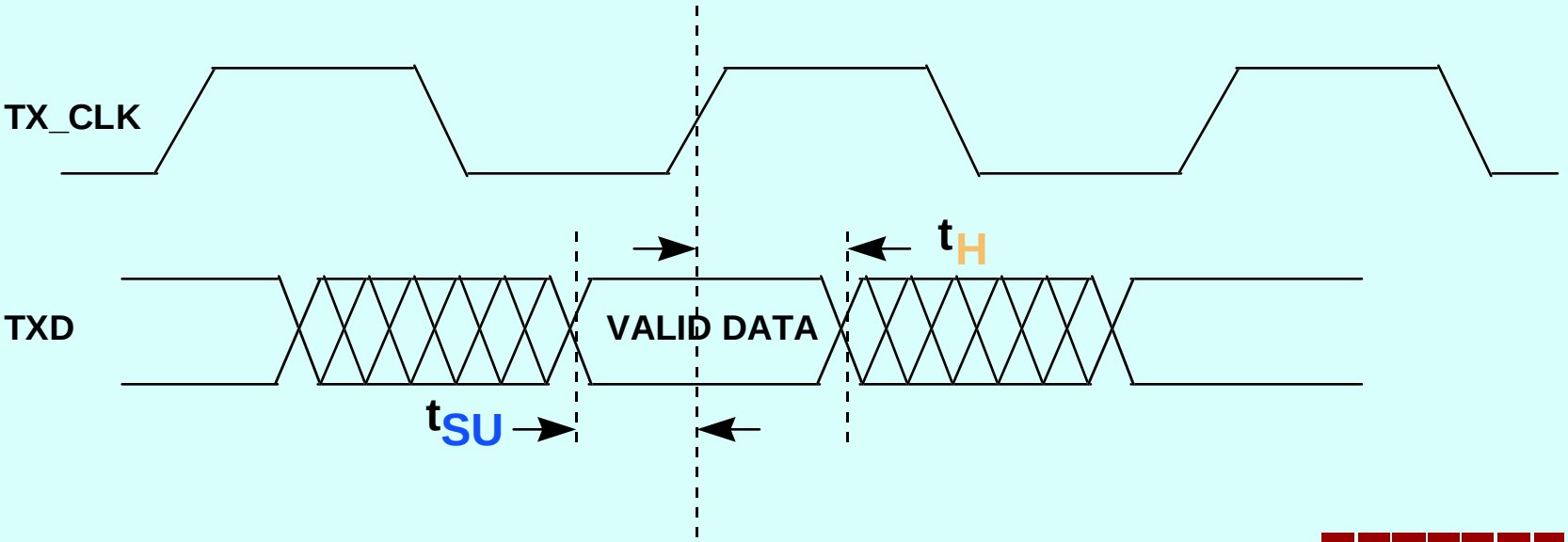
TX_EN	TX_CTRL	TXD<7:0>	Indication
0	0	00 through FFh	Normal inter frame
0	1	5Xh	Carrier extention
0	1	Otherwise	Reserved
1	0	00 through FFh	Normal data transmission
1	1	00 through FFh	Transmit error propagation

Gigabit MII - Permissible Encoding in Receive

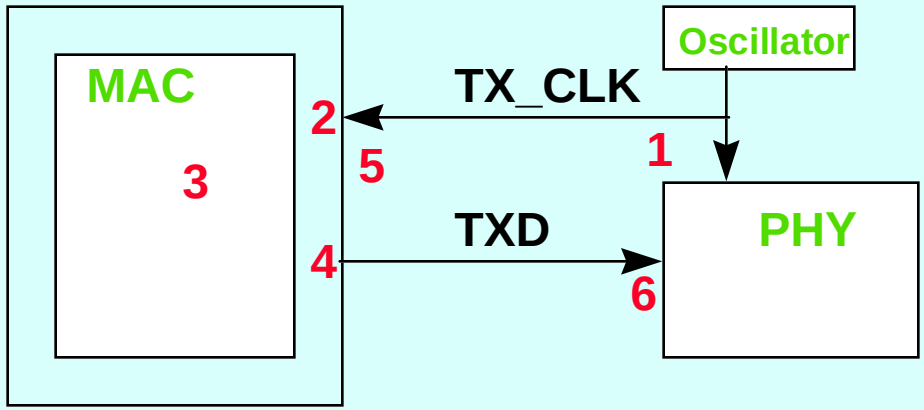
RX_DV	RX_CTRL	RXD<7:0>	Indication
0	0	00 through FFh	Normal inter frame
0	1	X0h	Normal inter frame
0	1	XEh	False carrier indication
0	1	5Xh (X <> 0,Eh)	Carrier extention
0	1	Otherwise	Reserved
1	0	00 through FFh	Normal data reception
1	1	00 through FFh	Data reception with errors

TX_CLK to TXD Path

- Assumptions (based on existing Fibre Channel Transceivers):
  - TXD setup time to the rising edge of TX_CLK: 2 nS min
  - TXD hold time after rising edge of TX_CLK: 1.5 nS min
  - TX_CLK rise and fall time: 1 nS max



TX_CLK to TXD Path Delays



1. Trace lines length
2. Clock input pad
3. Internal delay (data & clock)
4. Data output pad
5. Package model (PQFP)
6. PHY input capacitance

- Simulation done with Spice, Digital's 0.5 micron CMOS process

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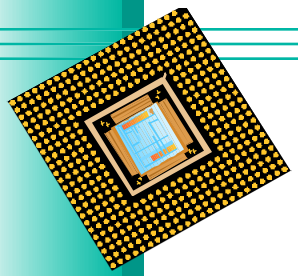
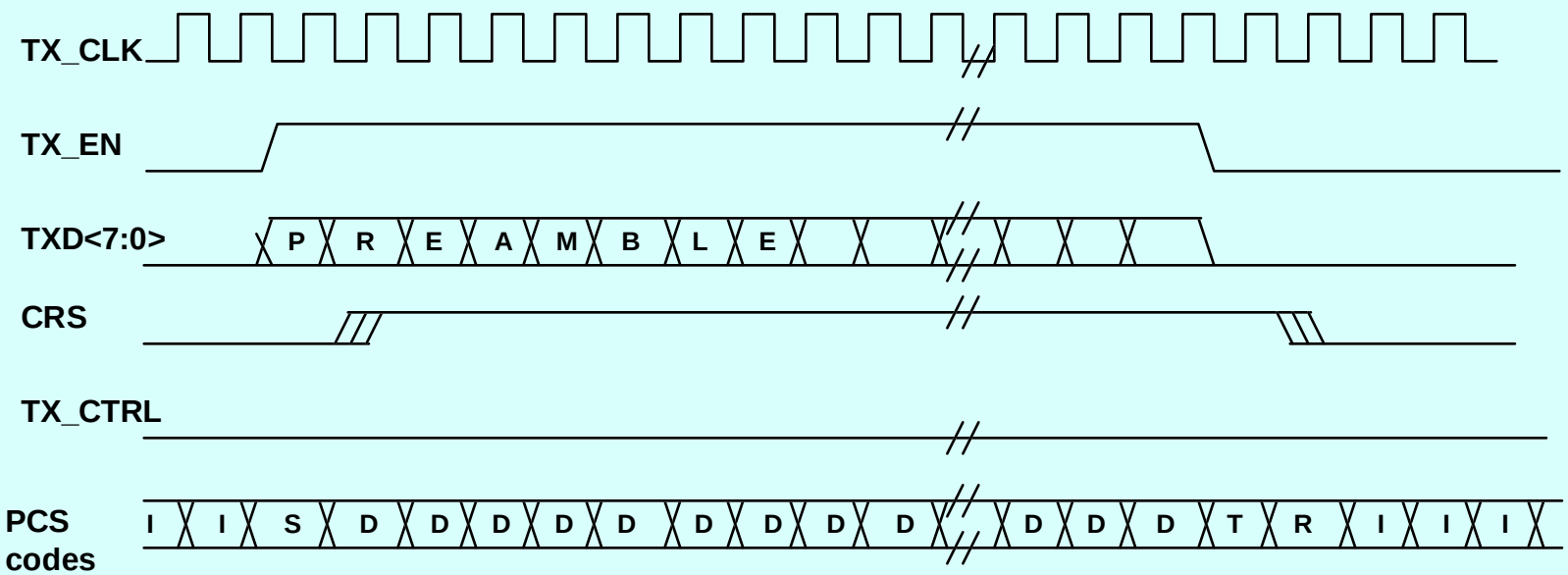


TX_CLK to TXD - Simulation

- Worst case for hold time
  - Trace lines length: 0.5 cm
  - Ideal clock (0 nS rise/fall time)
  - 3.465V, FF, 0 °C
  - PHY input capacitance: 5pF
- Worst case for setup time
  - Trace lines length: 8 cm
  - Clock rise/fall time: 1 nS
  - 3.135V, SS, 100 °C
  - PHY input capacitance: 5pF

Tx Gigabit MII and PCS codes
No Carrier Extention



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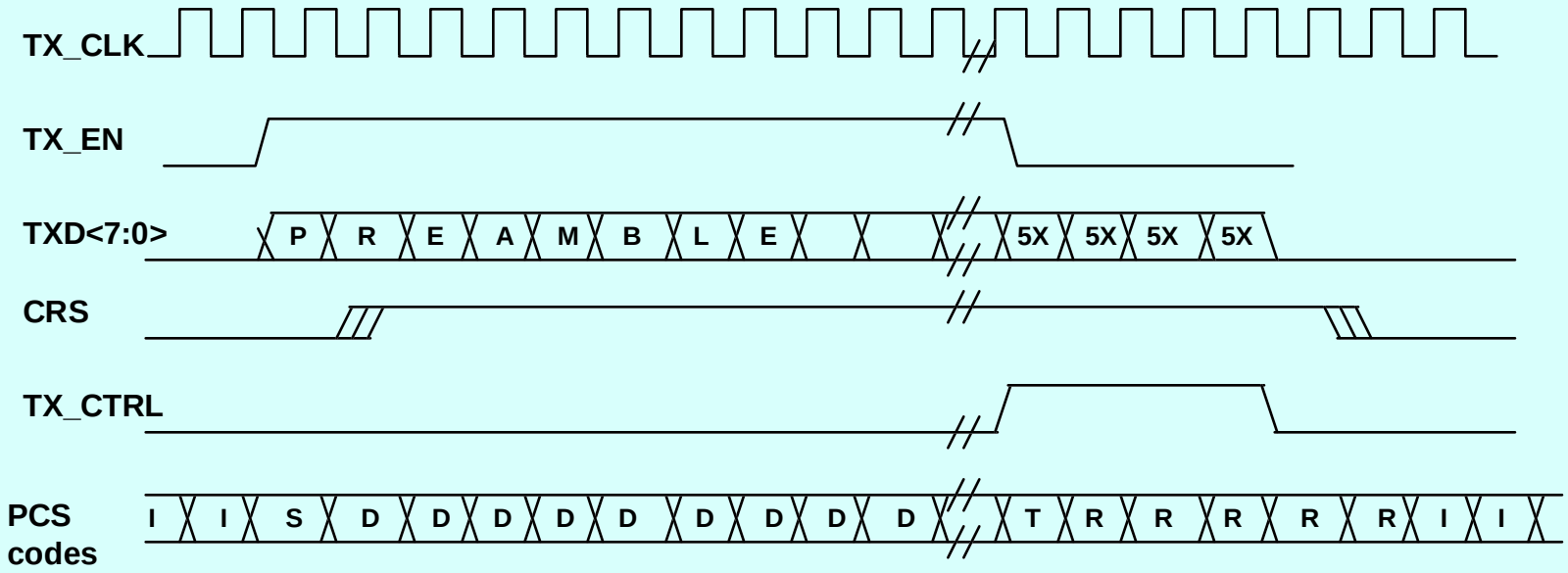
Tx Gigabit MII and PCS codes Carrier Extention



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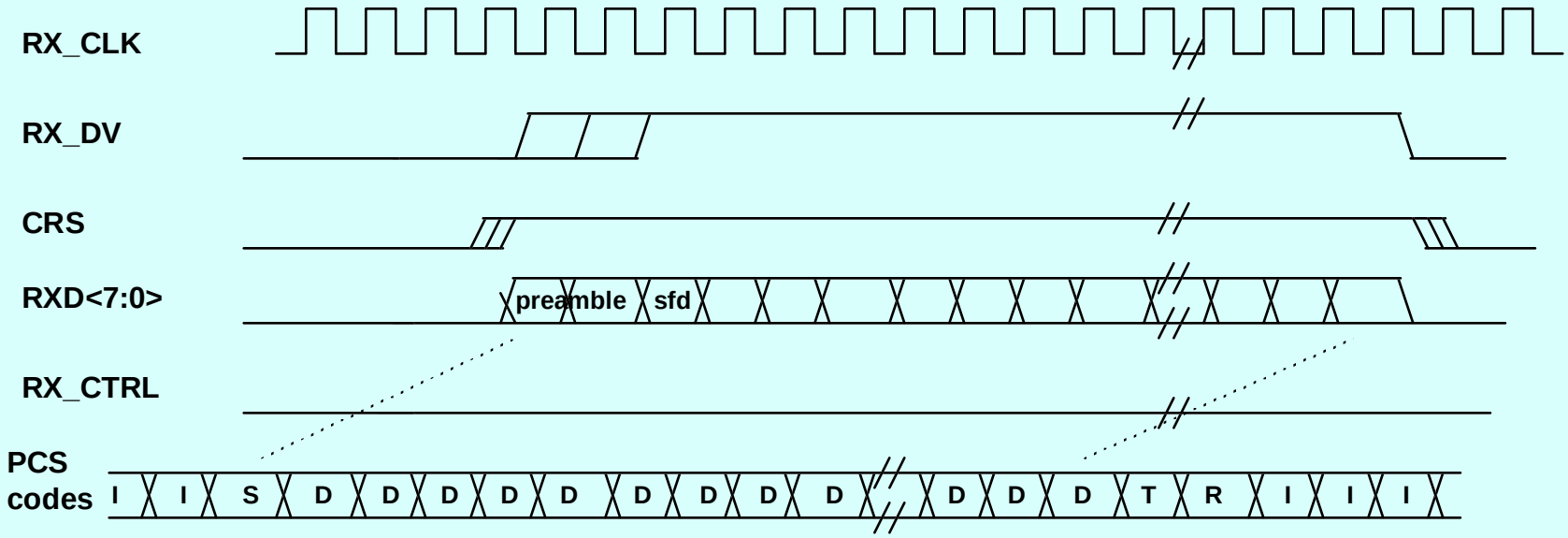
Rx Gigabit MII and PCS codes
No Carrier Extention



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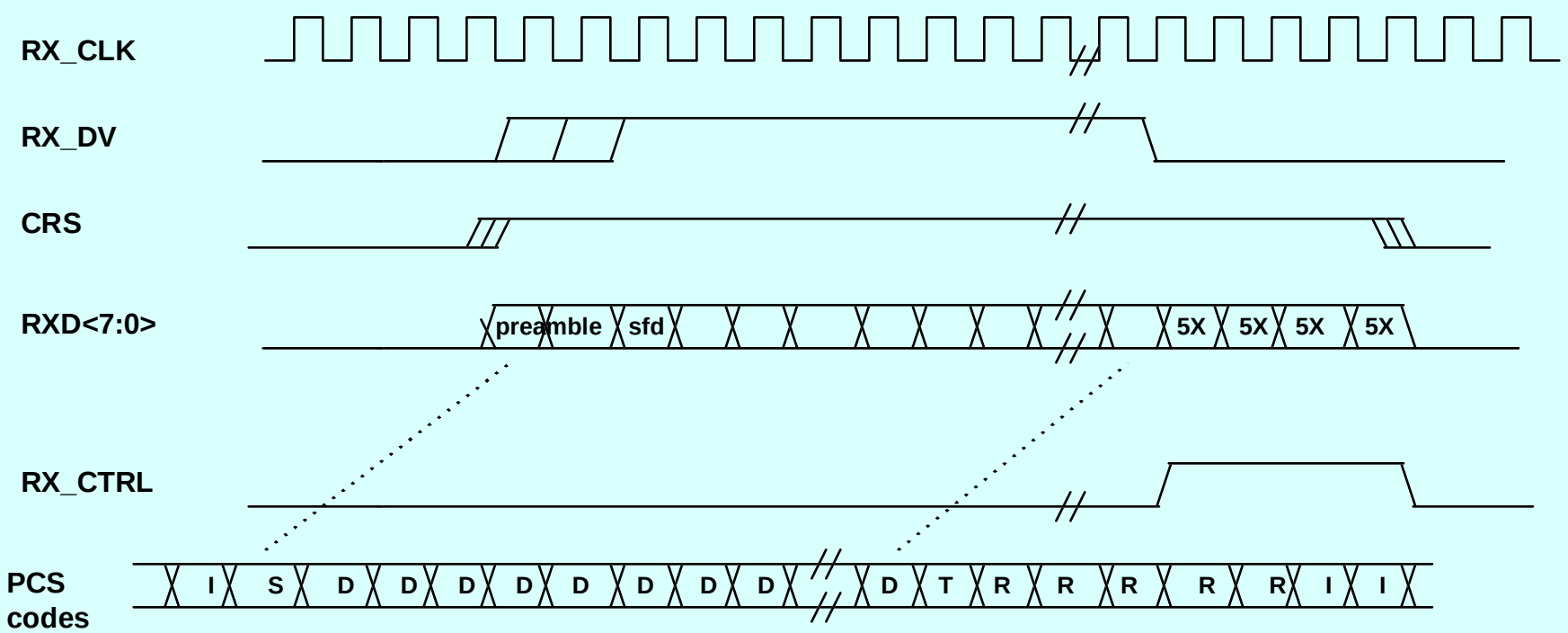
Rx Gigabit MII and PCS codes Carrier Extention



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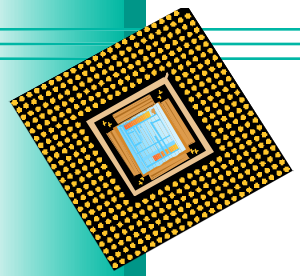
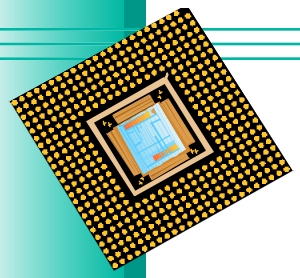


Advantages

- Very close to the 10/100 MII definition
  - Based on a proven working scheme
  - Most of the definition can be taken directly from 802.3u MII specification
- Allows control indication (CRS, COL) in parallel with the data
- Enables further extendibility
- Enables simple 10/100/1000 MAC implementations



Summary

- This presentation proposes:
  - A set of interface signals for Gigabit MII which are as close as possible to the 10/100 MII definition
  - Code for dealing with carrier extention