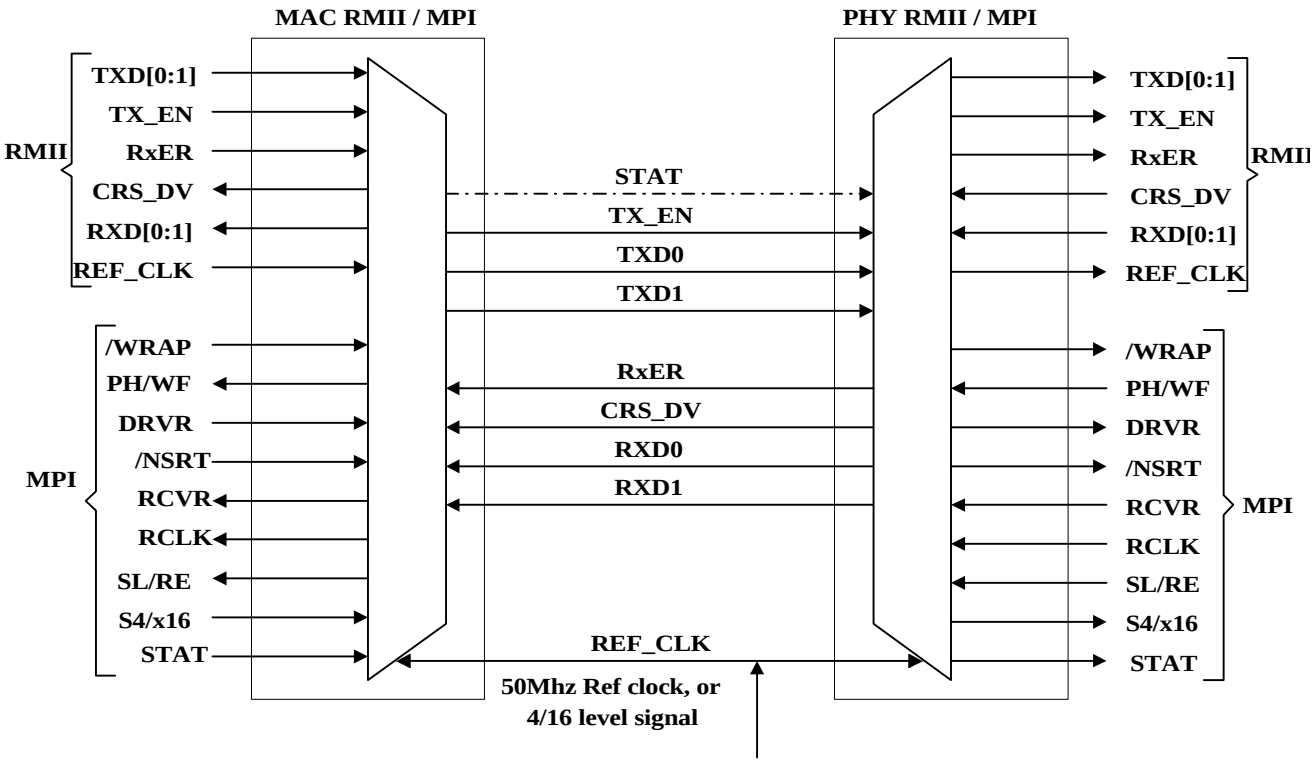
Proposal for HSTR/DTR common RMII/MPI

1.0 Overview

This document specifies a method to accommodate an implementation both for an HSTR RMII bus and a legacy DTR Mac PHY Interface (MPI). RMII is a standard low pin count MII that is targeted to lower the cost of multi port switches. The RMII is comprised of 6-7 pins per port, with a common synchronized clock signal for Rx and Tx data and control signals.

Figure 1: RMII and MPI signal map



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2.0 Signal Definition

The 7 fundamental RMII signal pins shall be used either in the original RMII method - supporting HSTR operation, or in the legacy Mac Processor Interface mode - supporting DTR16/4 mode. Mapping of data and control signals may be done according to items 1 - 7 of table 1. REF_CLK may be used as a speed signaling input that indicates HSTR operation (when toggling at 50Mhz), 16Mbps DTR when continuously pulled Low and 4Mbps DTR when continuously pulled High. The STAT function may be set using a dedicated pin that puts the port in ether Port mode or Station mode.
The STAT and Speed may also be defined via the out of band management.

Table 1: RMII and MPI signals

	RMII signal	**I/O**	**Use**	**DTR PHY signal**	**Use**
1	TX_EN	I	Transmit Enable	/WRAP	Port Wrap
2	CRS_DV	O	Transmit Error	PH/WF	Phantom Detect (port) or Wire Fault (Station)
3	TXD0	I	Transmit Data 0	DRVR	Transmit Data
4	TXD1	I	Transmit Data 1	/NSRT	Insert Phantom
5	RXD0	O	Receive Data 0	RCVR	Receive Data
6	RXD1	O	Receive Data 1	RCLK	Receive Clock
7	RX_ER	O	Receive Error*	SL/RE	Signal loss or Rate Error
8	REF_CLK	I/O	Sync clock for Rx/Tx**	S4/x16	Speed 4/16Mbps
9		I		STAT***	Port or Station mode

* The switch ASIC is not compelled to use this as an input
** May be only one per IC
*** Optional. Out of band management or another method may be used.

2.1 TX_EN (/WRAP)

Transmit Enable (HSTR); /WRAP (DTR)

In HSTR mode TX_EN indicates that the MAC is presenting di-bits on TXD[0:1] for transmission to the line. In DTR mode this signal is transformed into the /WRAP control line, moving the PHY to a WRAP (loopback) mode when Low, or to Normal data transmission mode when High.

2.2 CRS_DV (PH/WF)

Carrier Sense / Receive Data Valid (HSTR); Phantom/Wire Fault detect (DTR)

In HSTR mode CRS_DV is used by the PHY to signal the MAC that the receive medium is nonidle. Once CRS_DV is asserted the data on RXD[0:1] is considered valid. CRS_DV only means Data Valid in HSTR, as Carrier Sense is not applicable.

In DTR this signal is used by the PHY to indicate to the MAC that Phantom Current was detected (in port mode) or that a Wire Fault condition exists on the line (in Station Emulation mode).

2.3 TXD0 (DRVR)

Transmit data 0 (HSTR); Transmit data (DTR)

In HSTR mode TXD[0:1] transmit data from the MAC to the PHY, synchronously with REF_CLK. Data on TXD[0:1] is accepted by the PHY when TX_EN is asserted.

In DTR this signal is used to transmit data from the MAC to the PHY asynchronously and continuously.

2.4 TXD1 (/NSRT)

Transmit data 1 (HSTR); Insert Phantom (DTR)

In HSTR mode TXD[0:1] transmit data from the MAC to the PHY, synchronously with REF_CLK. Data on TXD[0:1] is accepted by the PHY when TX_EN is asserted.

In DTR mode the MAC uses this signal to request assertion of the Phantom from the PHY, to test the line for Wire Fault condition.

2.5 RXD0 (RCVR)

Receive Data 0 (HSTR); Receive Data (DTR)

In HSTR mode RXD[0:1] transmit data from the to PHY the MAC, synchronously with REF_CLK. Data on RXD[0:1] is considered valid by the MAC when CRS_DV is asserted.
In DTR mode RCVR is the data transmitted from the PHY to the MAC synchronously with RCLK, being the clock recovered from data on the line by the PHY.

2.6 RXD1 (RCLK)

Receive Data 1 (HSTR); Receive Clock (DTR)

In HSTR mode RXD[0:1] transmit data from the to PHY the MAC, synchronously with REF_CLK. Data on RXD[0:1] is considered valid by the MAC when CRS_DV is asserted.

In DTR mode RCLK is the clock recovered from the data on the line by the PHY.

2.7 RXER (SL/RE)

Receive Error (HSTR); Signal Loss/Rate Error (DTR)

In HSTR mode RXER is asserted for one or more REF_CLK periods to indicate that an Error was detected by the PHY in the frame presently being transferred. The MAC ignores RXER while CRS_DV is not asserted.

In DTR mode SL/RE indicates the MAC that the PHY has detected a Signal Loss or a Rate Error condition. The PHY indicates a Signal Loss condition by de-asserting SL/RE altogether and Rate Error by toggling SL/RE every X μs, synchronously to RCVR.

2.8 REF_CLK (S4/x16)

Reference Clock (HSTR); Speed 4 / 16Mbps (DTR)

In HSTR mode REF_CLK is a continuous clock that provides the timing reference for RXD[0:1], TXD[0:1], CRS_DV, TXEN and RE_ER. REF_CLK is sourced by the MAC or asserted for one or by an external source. The standard allows a PHY device to have a single REF_CLK input for multiple PHY ports on the same IC.

In DTR mode S4/x16 is an input to the PHY device that defines the data rate it should operate in – 4Mbps or 16Mbps. When this line is de-asserted the speed is set to 16Mbps and when it is asserted the speed is set to 4Mbps.

The PHY devise remains in HSTR mode while this signal is toggled at a rate higher then 1MHz. Otherwise, it moves to DTR mode, and defines the speed according to this signal level.

2.9 STAT

Port mode or Station Emulation mode (DTR only mode)
When STAT is asserted the port is in Station mode, and when STAT is de-asserted, it is in port mode.

This information may be communicated to the PHY device via the STAT pin, or out of band management. A third method can be defined, multiplexing it on one of the other inputs to the PHY (/WRAP or /NSRT), eliminating the need for a dedicated STAT pin.